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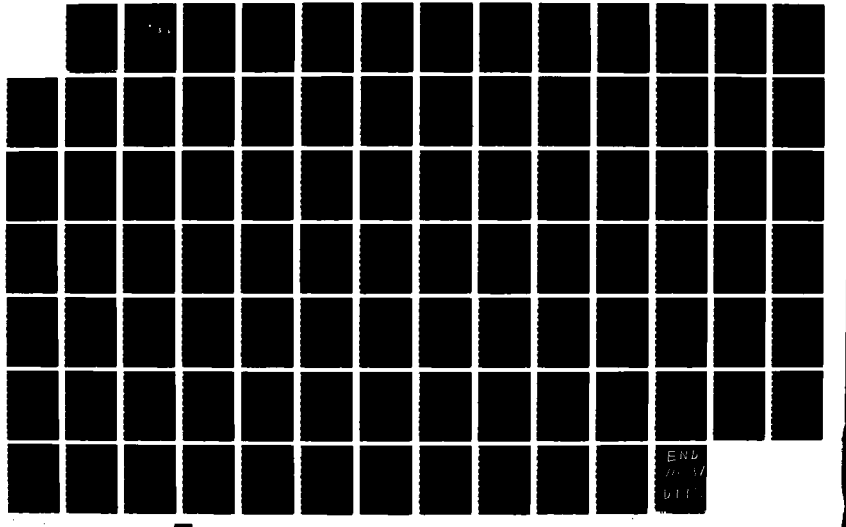

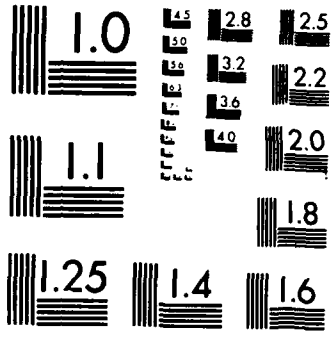

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NAVAL POSTGRADUATE SCHOOL

Monterey, California

THESIS

EVALUATION OF DEVICE FIGURE OF MERIT
IN
MICROWAVE SWITCHING CIRCUIT DESIGN

by

Pitak Pibultip

June 1987

Thesis Advisor H.A. Atwater

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Evaluation of Device Figure of Merit
in
Microwave Switching Circuit Design

by

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Submitted in partial fulfillment of the
requirements for the degree of

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ABSTRACT

In microwave switching circuit design, a switching-semiconductor figure of merit can be defined and used as the measure of device switching effectiveness. In this thesis research switching-semiconductor figures of merit were applied to general switching circuits. Computer-aided circuit analysis program (Touchstone), and a Fortran program were used for the computation of switching circuit performance.

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I. INTRODUCTION

A. BACKGROUND

The switching function as performed in microwave circuitry utilized in radar applications is essential for the performance of the circuit objective. In the majority of practical cases, switching must be done by semiconductor devices, since mechanical switches are ruled out by requirements of speed and allowable system weight and size. Therefore the semiconductor switch is a vital component in most microwave circuit applications.

Despite its practical importance, relatively little research attention has been given to fundamental aspects of the switching problem, in comparison with, for example, the problem of microwave amplifier or filter design. Therefore it is the purpose of this thesis to examine some of the basic features of the switching problem. A general requirement in the design of a switching circuit is the conversion of the set of given switch performance specifications into a set of device requirements for the necessary semiconductors to be used in the switch. It is known that a device figure of merit can be defined which provides a unifying factor in this conversion process. Some progress in the definition and use of switch figures of merit has been made by earlier workers, but few practical procedures have been developed, and further work is needed in this area. It is the purpose of this thesis to investigate the characterization of several aspects of switch performance as a function of device figure of merit, as well as to investigate the important aspect of the selection and use of devices so as to maximize the power-handling capacity of the switch.

The fundamental specifications governing microwave switch selection and/or design are:

1. Low insertion loss in on-state
2. High isolation in off-state
3. Broad bandwidth
4. Sufficient power capability

These characteristics are interactive, a change in one affecting the others. The microwave switches considered here are those which employ semiconductor devices (p-i-n diodes and FET's) operated in two alternate bias states. The device is characterized by a pair of two-terminal impedance values Z_1 and Z_2 in the respective

bias states. The parasitic capacitance associated with semiconductor switching devices necessitates some form of impedance compensation in order to achieve acceptable insertion losses for the switch. Consequently the theoretical analysis of switching circuitry has been oriented toward the study of two-state impedances embedded in lossless impedance transformers [Refs. 1,2,3]. These researches on switching theory have introduced specific invariant parameters related to the device impedance in its two states, under lossless impedance transformation.

Kurokawa and Schlosser [Ref. 1], showed that diodes incorporated in a one-port reflective switch can be characterized by a quality factor parameter, Q^2 :

$$Q^2 = \frac{|Z_1 - Z_2|^2}{R_1 R_2} \qquad \text{(eqn 1.1)}$$

where R_1 is the resistive component of Z_1, and

R_2 is the resistive component of Z_2.

The numerical value of Q is unchanged when the impedances are subjected to a lossless impedance transformation.

Atwater and Sudbury [Ref. 2] showed that this Q had the character of a figure of merit, serving as an indicator of switching performance for semiconductors embedded in variety of circuit configurations, and not restricted to the original reflection-type circuit of Kurokawa and Schlosser. They followed the research of Kurokawa and Schlosser and assumed that Z_1 and Z_2 had been transformed to real (resistive) values in both states. Equation 1.1 becomes:

$$Q^2 = \frac{[R_1 - R_2]^2}{R_1 R_2} \qquad \text{(eqn 1.2)}$$

From equation 1.2, we have the relationships:

R_1 is a function of Q and R_2, and

R_2 is a function of Q and R_1.

Knowing the value of Q and given that R_1, R_2 are known, the switching performance is fully specified.

Kawakami [Ref. 3] found a different form of switching invariant parameter. He defined this parameter as a semiconductor figure of merit, M:

$$M = \frac{|Z_1 - Z_2|}{Z_1 + Z_2^*} \qquad \text{(eqn 1.3)}$$

The parameter M assumes values between 0 and 1, and is also unaltered by lossless impedance transformation. Kawakami also showed that when a device was incorporated in a symmetrical two-port junction as a switch, its transmission coefficients in the on and off states, $S_{21}(1)$ and $S_{21}(2)$, respectively, are related by equation:

$$|S_{21}(2)| = \frac{|S_{21}(1)|(1-M)}{1-M\,[|1-2\,S_{21}(1)|]} \qquad \text{(eqn 1.4)}$$

Equation 1.4 fully characterizes the switching performance of the device, with parameter M as a figure of merit. It may inverted to yield the form:

$$M = \frac{|S_{21}(2)| - |S_{21}(1)|}{|S_{21}(2)| + |S_{21}(1)|\,[|1-2|S_{21}(2)|]} \qquad \text{(eqn 1.5)}$$

This expression is based on the assumption that the switching device in its two states has the properties:

$$\Gamma_1 = 0 \text{ (matched; } Z = Z_0 \text{)}$$

$$\Gamma_2 = \Gamma_{max} = M$$

Equation 1.5 presents a useful tool for the selection of a semiconductor device to satisfy low power switching applications.[1]

A fundamental theorem was derived by Hines [Ref. 4], to predict the power that can be switched by a single-diode switch when it is connected in a lumped-element circuit such as to resonate the parasitic reactance of the switch at a single frequency. Hines showed that the power which can be switched by the diode, P_{sw}, is given by:

---

[1] In the absorption switch assumed in equation 1.4, the diode absorbs the incident energy in the switch off-state.

$$P_{sw} = 0.5[V_{max}I_{max}] \quad \text{(eqn 1.6)}$$

where V_{max} is a diode breakdown voltage, and

I_{max} is a maximum forward current rating.

Hines conjectured that P_{sw} represents a theoretical limit for power switching by a given device in an impedance-matched circuit.

In many applications, microwave switching circuits typically require multiple diodes in cascade connection to achieve adequate levels of off-state isolation. For example, radar and phased-array modules need a double-throw switch of high isolation to protect the receiver front end.

B. SCOPE OF THE THESIS RESEARCH

For the application to microwave switching, the proposed semiconductor figures of merit are tested for different types of switching circuitry, to find the best parameter to use in a switch selection and/or design problem in order to minimize insertion loss in the on-state, and maximize isolation in the off-state. Additional objectives are to determine, for the designed switch, what are the power dissipation and heat removal problem in the individual semiconductor components.

II. CIRCUIT ANALYSIS

In the present chapter we generalize the circuit representation of microwave switches of our interest. Following this, a suitable circuit model may be selected for the particular type of switch required. The simplest representation is that of an N-port, with scattering matrix description. The number of ports is determined by the number of semiconductor devices and the type of switch (single-throw or multiple-throw). For the semiconductor devices, there are three possible ways of connection to our circuit model, in shunt or in series or a combination of both. Because of heat-sinking considerations we select the shunt connection and use a one-port network to represent the two-terminal semiconductor device.

A. CLASSIFICATION OF MICROWAVE SWITCHES

1. Single Pole Single Throw Switches (SPST)

The single pole[2] single throw switch is a switch which has one input port and one output port. In this topology we consider our switch as a 'box' and it is a two-port box network shown in Figure 2.1(a). For an ideal switch, all the power is transferred to the load at the output port in its on-state, and no power transferred to the load in its off-state.

2. Single Pole N Throw Switches (SPNT)

For these types of switches, there is an input port and N output ports. Their switching circuit models are a three-port box network for single pole double throw switches, shown in Figure 2.1(b), and a (N+1)-port box network for single pole N-throw switches, shown in Figure 2.1(c). In microwave switch application, we are interested in single pole double throw switches as mentioned in the introductory chapter. For SPDT switches, when one arm of the switch is in the on-state, the other arm is in the off-state, and vice versa. In general, we may consider a SPDT switch as two SPST switches with their input arms tied together and apply two different bias states to the semiconductor devices in the different arms of the switch.

---

[2]Single pole is a line-over-ground circuit.

B. SCATTERING MATRIX REPRESENTATION OF MICROWAVE SWITCHES

We can use the properties of the S-matrix [Refs. 5,6: pp. 112, 50], defined in Figure 2.2, and assume that our switches are ideal switches with matched load at both input and output ports. We can represent the scattering matrices for both on and off states of our switches as follows.

1. Single Pole Single Throw Switch

$$\text{ON STATE: } [S] = \begin{bmatrix} 0 & 1 \\ 1 & 0 \end{bmatrix}$$

$$\text{OFF STATE: } [S] = \begin{bmatrix} 1 & 0 \\ 0 & 1 \end{bmatrix}$$

2. Single Pole Double Throw Switch

$$\text{ARM (2) ON: } [S] = \begin{bmatrix} 0 & 1 & 0 \\ 1 & 0 & 0 \\ 0 & 0 & 0 \end{bmatrix}$$

$$\text{ARM (3) ON: } [S] = \begin{bmatrix} 0 & 0 & 1 \\ 0 & 0 & 0 \\ 1 & 0 & 0 \end{bmatrix}$$

C. SWITCHING CIRCUIT MORPHOLOGIES

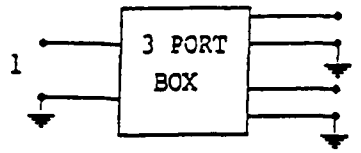
1. Number of Semiconductor Devices

In an SPST switch or one arm of SPDT switch there is at least one semiconductor device. For improvement of load isolation, the switch may require additional semiconductor devices. In general, a SPNT switch may use M semiconductor devices.

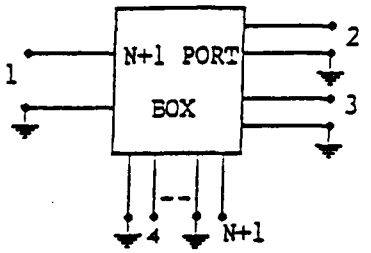
$$M = \rho N \qquad \text{eqn 2.1}$$

where M is the number of semiconductor devices,
N is the number of throws, and
ρ is a positive integer.

a. SPST

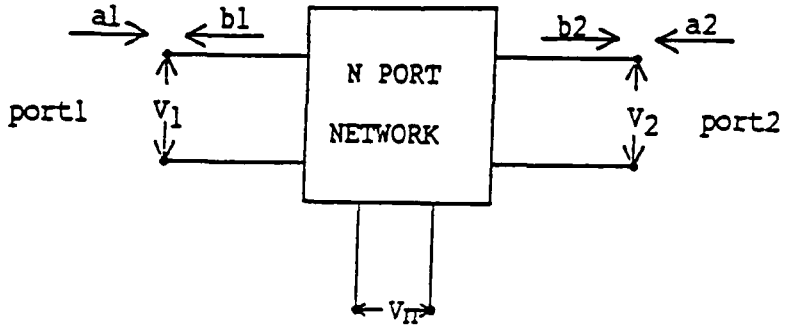


b. SPDT



c. SPNT

Figure 2.1 Single Pole N Throw Switches.



$$[b] = [S][a]$$

That is

$$b_1 = S_{11}a_1 + S_{12}a_2 + \text{---} + S_{1n}a_n$$

$$b_n = S_{n1}a_1 + S_{n2}a_2 + \text{---} + S_{nn}a_n$$

Figure 2.2 Scattering Parameters.

2. **Switch "BOX" Topologies**

We can define the switching circuit as a lossless embedding network with one input port, N output ports, and M ports to which the semiconductor devices are coupled. The total number of ports of the embedding network is given by:

$$\text{Number of ports} = (N+1+M) \qquad \text{(eqn 2.2)}$$

Example of switching circuits.

1. SPST switch with 1 semiconductor device. Figure 2.3(a)

   Number of ports = (1+1+1)

   = 3 ports

2. SPST switch with 2 semiconductor devices. Figure 2.3(b)

   Number of ports = (1+1+2)

   = 4 ports

3. SPDT switch with 2 semiconductor devices. Figure 2.3(c)

   Number of ports = (2+1+2)

   = 5 ports

D. SWITCHING SEMICONDUCTOR DEVICE CHARACTERIZATION

The semiconductor device in shunt connection can be represented by a one-port network, as stated above.[3] The device itself in the switching circuit may be characterized by:

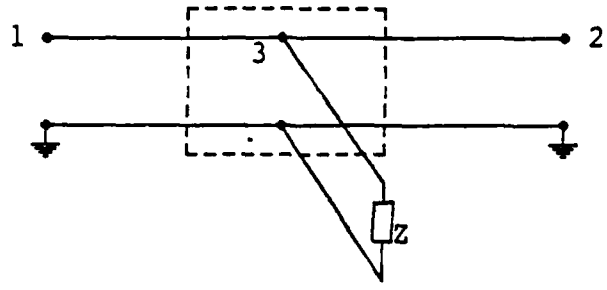
1. Two-states of impedance [Ref. 2]. Z_i (i = 1,2) or
2. Two-states of reflection coefficient [Ref. 1]. Γ_i (i = 1,2).

The relations between impedance and reflection coefficient are:

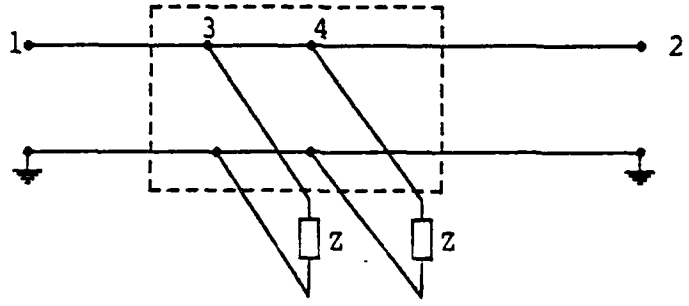
$$Z_i = \frac{1 + \Gamma_i}{1 - \Gamma_i} Z_0 \qquad \text{(eqn 2.3)}$$

$$\Gamma_i = \frac{Z_i - Z_0}{Z_i + Z_0} \qquad \text{(eqn 2.4)}$$

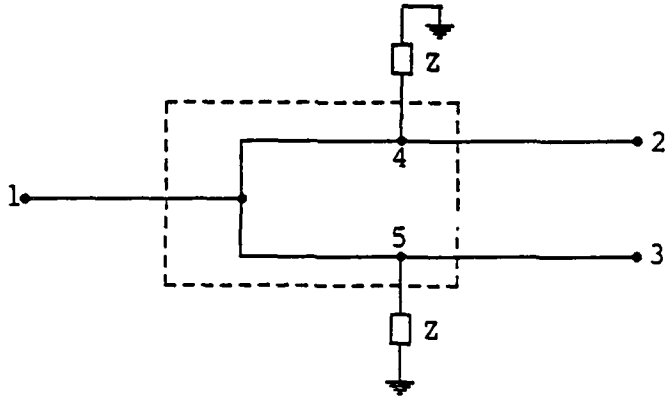
[3]The device is in shunt to ground in the single pole circuit.



a. SPST 1 DEVICE



b. SPST 2 DEVICES



c. SPDT 2 DEVICES

Figure 2.3 Example of Switching Circuits.

Figure of merit of the semiconductor device is defined based on the device characterization chosen.

1. **Figure of Merit, M**

From equation 1.3

$$M = \frac{|Z_1 - Z_2|}{|Z_1 - Z_2^*|}$$

Kawakami postulated that the fundamental characterization was in terms of two specific states of Γ_i. He assumed the following conditions:

$$\Gamma_1 = 0 \quad (Z \text{ is matched; } Z = Z_0)$$

A lossless matching network is assumed to be used to transform the device impedance to the matched condition in this state. In the second bias state of the device, the reflection coefficient presented by the transformed device impedance is then:

$$|\Gamma_2| = |\Gamma_{max}| \text{ (this is equal to the figure of merit, M, of the devices)}$$

However, this type of switch is a reflection switch.[4]

2. **Quality Factor, Q**

Kurokawa and Schlosser postulated that the fundamental characterization was in terms of two states of impedance and their real parts (resistive). They defined a quality factor Q^2, shown in equation 1.1, as the figure of merit of the semiconductor devices.

From the parameters defined above we can characterize the p-i-n diode and specify a diode quality factor or the figure of merit for the device used in microwave switching circuits. Diode quality factor, Q_{diode}, for a typical switching diode is equal to the switching quality factor, as may be shown:

From equation 1.1

$$Q^2 = \frac{(R_1 - R_2)^2 + (X_1 - X_2)^2}{R_1 R_2}$$

---

[4]The $\Gamma_i = 0$ state, absorbs energy and is not suitable for high power switching circuits.

For a p-i-n diode, a simple circuit model is assumed in which the two impedance states are:

$$Z_1 = R_1 \qquad \text{forward bias}$$
$$Z_2 = R_2 + jX_2 \qquad \text{reverse bias}$$

If we assume that $R_1 = R_2 = R$ (for both bias states)

$$Q^2 = \frac{|X_2|^2}{R^2}$$
$$= \frac{1}{(RC\omega)^2}$$

Thus Kurokawa-Schlosser's Q reduces to the conventional diode Q:

$$Q^2 = Q^2_{diode} \qquad \text{(eqn 2.6)}$$

3. Comparison of Figure of Merit

We can find the relationships between the figure of merit, M, and the quality factor, Q, as follows:

Kurokawa-Schlosser, quality factor, from equation 1.1

$$Q^2 = \frac{|Z_1 - Z_2|^2}{R_1 R_2}$$
$$Q^2 = \frac{(R_1-R_2)^2 + (X_1-X_2)^2}{R_1 R_2} \qquad \text{(eqn 2.7)}$$

Kawakami, figure of merit, from equation 1.3

$$|M|^2 = \frac{|Z_1 - Z_2|^2}{|Z_1 + Z_2^*|^2}$$
$$|M|^2 = \frac{(R_1 - R_2)^2 + (X_1 - X_2)^2}{(R_1 + R_2)^2 + (X_1 - X_2)^2} \qquad \text{(eqn 2.8)}$$
$$\frac{1}{1 - |M|^2} = \frac{1}{1 - \frac{|Z_1 - Z_2|^2}{|Z_1 + Z_2^*|^2}}$$

$$= \frac{|Z_1 + Z_2^*|^2}{|Z_1 + Z_2^*|^2 - |Z_1 - Z_2|^2}$$

$$= \frac{|Z_1 + Z_2^*|^2}{4R_1R_2}$$

$$= \frac{Q^2}{4|M|^2}$$

$$Q^2 = 4\frac{|M|^2}{1 - |M|^2} \qquad \text{(eqn 2.9)}$$

$$|M|^2 = \frac{Q^2}{4 + Q^2} \qquad \text{(eqn 2.10)}$$

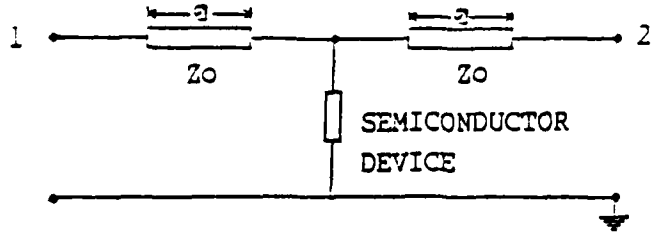
If $Q^2 >> 1$

$$|M| \cong 1 - \frac{2}{Q^2} \qquad \text{(eqn 2.11)}$$

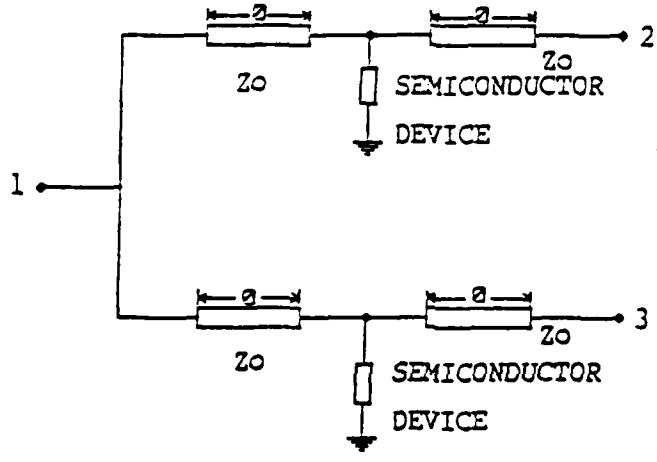
E. TRANSMISSION LINE SECTION REPRESENTATION OF SWITCHING CIRCUIT MODEL

From an N-port box representation, the semiconductor devices are in shunt to ground and have two alternate impedance values. For practical microwave integrated circuit (MIC) applications, it is convenient to use transmission line sections in the embedding network of the switches

Figure 2.4, shows the circuit model of SPST and SPDT switches with one semiconductor device in each arm. To optimize the switch characteristics for low insertion loss and high isolation, the impedance values of the devices are kept unchanged at the particular frequency in each state. The length and characteristic impedance of the transmission line section are varied to achieve the optimum switching characteristics in a particular frequency interval.



SPST 1 DEVICE



SPDT 2 DEVICES

θ = Transmission Line Electrical Length

Zo = Transmission Line Characteristic Impedance

Figure 2.4 Transmission Line Model of Switch Networks.

F. APPROACHES TO COMPUTATION OF CIRCUIT POWER-DISSIPATION

Using the Touchstone program, we can design a switch to have optimum switching characteristics. But the semiconductor devices in the optimized circuit may not be able to handle the amount of power dissipated due to heating of the devices. For effective switching design, it is advisable to calculate the maximum power dissipation in each device before construction of the switch.

1. ABCD Matrix Representation of a Two-port Network

From Figure 2.5 the ABCD matrix is defined in equations 2.12 and 2.13

$$V_1 = AV_2 + BI_2 \qquad \text{(eqn 2.12)}$$

$$I_1 = CV_2 + DI_2 \qquad \text{(eqn 2.13)}$$

Equations 2.12 and 2.13 have the matrix form.

$$\begin{bmatrix} V_1 \\ I_1 \end{bmatrix} = \begin{bmatrix} A & B \\ C & D \end{bmatrix} \begin{bmatrix} V_2 \\ I_2 \end{bmatrix} \qquad \text{(eqn 2.14)}$$

$$\begin{bmatrix} V_2 \\ I_2 \end{bmatrix} = \begin{bmatrix} A & B \\ C & D \end{bmatrix}^{-1} \begin{bmatrix} V_1 \\ I_1 \end{bmatrix}$$

$$= \begin{bmatrix} D & -C \\ -B & A \end{bmatrix} \begin{bmatrix} V_1 \\ I_1 \end{bmatrix} \qquad \text{(eqn 2.15)}$$

The utility of the general circuit parameter matrix lies in the fact that cascaded two-ports can be represented by the chained product of element matrices [Ref. 5: p 110].

$$\begin{bmatrix} V_1 \\ I_1 \end{bmatrix} = \begin{bmatrix} A_1 & B_1 \\ C_1 & D_1 \end{bmatrix} \begin{bmatrix} A_2 & B_2 \\ C_2 & D_2 \end{bmatrix} \cdots\cdots \begin{bmatrix} A_n & B_n \\ C_n & D_n \end{bmatrix} \begin{bmatrix} V_{n+1} \\ I_{n+1} \end{bmatrix} \qquad \text{(eqn 2.16)}$$

Thus the general circuit parameter matrix representation of cascaded two-ports is the matrix product of general circuit parameter matrices of the individual two-ports, as shown in Figure 2.6.

2. ABCD Matrix Representation of the Switching Circuit Model

In the circuit model we have transmission line sections and semiconductor devices combined. Lumped-circuits can be characterized by ABCD two-port matrices [Ref. 7: p. 188], as follows:

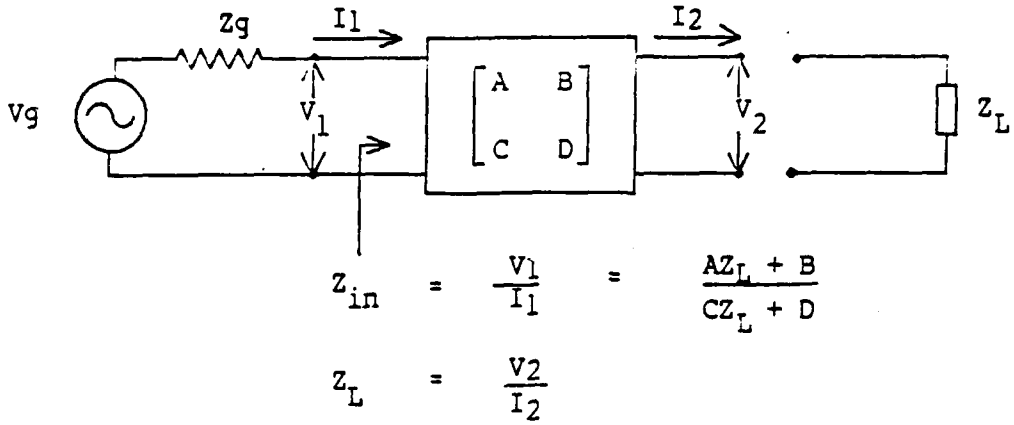


Figure 2.5 ABCD Matrix Model.

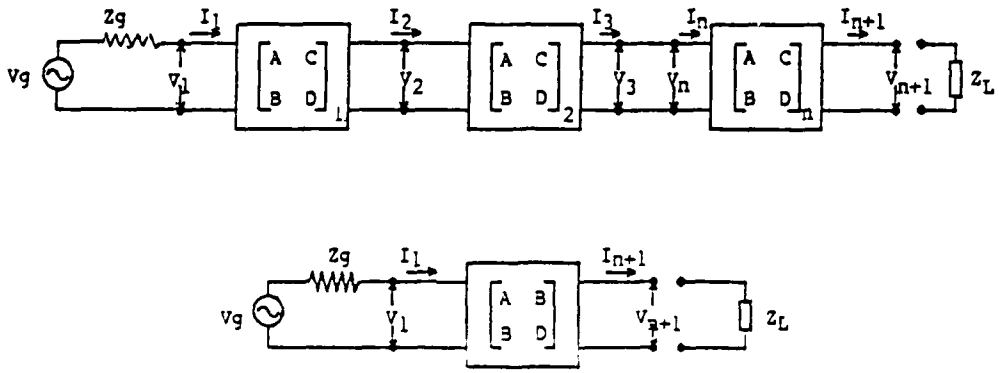


Figure 2.6 N Two-Port in Cascade with Equivalent Matrix.

2.1 Series impedance, as shown in Figure 2.7 (a)

$$\begin{bmatrix} A & B \\ C & D \end{bmatrix} = \begin{bmatrix} 1 & Z \\ 0 & 1 \end{bmatrix} \qquad \text{(eqn 2.17)}$$

2.2 Shunt admittance, as shown in Figure 2.7 (b)

$$\begin{bmatrix} A & B \\ C & D \end{bmatrix} = \begin{bmatrix} 1 & 0 \\ Y & 1 \end{bmatrix} \qquad \text{(eqn 2.18)}$$

2.3 Lossless transmission line section, as shown in Figure 2.7 (c)

$$\begin{bmatrix} A & B \\ C & D \end{bmatrix} = \begin{bmatrix} \text{Cos}\theta & jZ_0\text{Sin}\theta \\ jY_0\text{Sin}\theta & \text{Cos}\theta \end{bmatrix} \qquad \text{(eqn 2.19)}$$

θ is an electrical length of a transmission line section

2.4 Lossy transmission line section, as shown in Figure 2.7 (d)

$$\begin{bmatrix} A & B \\ C & D \end{bmatrix} = \begin{bmatrix} \text{Cosh}(\gamma\, l) & Z_0\text{Sinh}(\gamma\, l) \\ Y_0\text{Sinh}(\gamma\, l) & \text{Cosh}(\gamma\, l) \end{bmatrix} \qquad \text{(eqn 2.20)}$$

l = Physical length of a transmission line section.

$\gamma = \alpha + j\beta$

α = transmission line attenuation constant.[5]

β = wavenumber.

3. **Calculation of Power in a Cascade Circuit**

From Figures 2.5, and 2.6 [Ref. 8: p. 393].

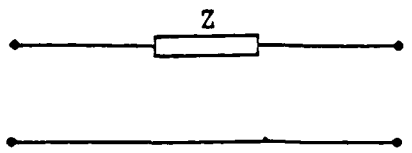
$$Z_{in} = \frac{AZ_L + B}{CZ_L + D} \qquad \text{(eqn 2.21)}$$

$$I_1 = \frac{V_g}{Z_g - Z_{in}} \qquad \text{(eqn 2.22)}$$

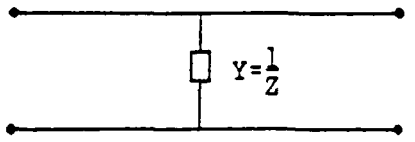
$$V_1 = \frac{Z_{in}}{Z_g + Z_{in}} V_g \qquad \text{(eqn 2.23)}$$

$$I_{j+1} = (A_j I_j) - (C_j V_j) \qquad \text{(eqn 2.24)}$$

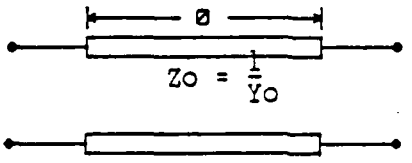
[5] $\alpha = 0$ for a lossless transmission line section.



a. SERIES IMPEDANCE

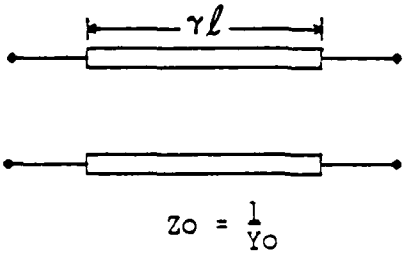


b.SHUNT ADMITTANCE



ø =ELECTRICAL LENGTH

c.LOSSLES TRANSMISSION LINE SECTION



d.LOSSY TRANSMISSION LINE SECTION

Figure 2.7 ABCD Matrix Representation of Devices.

$$V_{j+1} = (D_j V_j) - (B_j I_j) \qquad \text{(eqn 2.25)}$$

$j = 1,2,3,.....,n$

Power dissipated in each two-port network.

$$P_k = 0.5\,\mathcal{R}e\,[(V_k I_k^*) - (V_{k+1} I_{k+1}^*)] \qquad \text{(eqn 2.26)}$$

$k = 1,2,3,.....,n$

Power at load

$$P_L = 0.5\,\mathcal{R}e\,[V_{n+1} I_{n+1}^*] \qquad \text{(eqn 2.27)}$$

$$= P_{in} - \sum_{k=1}^{n} P_k \qquad \text{(eqn 2.28)}$$

III. MICROWAVE SWITCHING DIODE

The use of the semiconductor diode as a switching element in microwave circuits is based on the difference between the diode impedance under reverse and forward bias. The diode appears as a very small impedance under forward bias and a very large impedance under reverse bias. For a shunt-connected diode as a microwave switch, in its on state most of the power is delivered to the load, and the diode looks like a large impedance (reverse bias state). On the other hand, in its off state, the power is reflected back to the source, or dissipated in the diodes, and the diodes look like a small impedance (forward bias state) in shunt to ground. In this chapter we will introduce some characteristics of the p-i-n diode, its behavior under forward and reverse bias states, the equivalent circuit, and power handling capability.

A. THE P-I-N DIODE STRUCTURE

In a p-i-n diode, the semiconductor wafer has a heavily doped P-region and a heavily doped N-region separated by a layer of high resistivity material that is nearly intrinsic. The thickness of the high resistivity layer lies in the range between 1.5 to 150 microns [Ref. 9: p. 5]. The electrical contacts are made to the two heavily doped regions.

In practice, there are no materials without any impurities. A practical p-i-n diode consists of extremely high resistivity P or N-type material between low resistivity (highly doped) P and N-regions. The lightly doped, high resistivity layer is called π-type for P material, and ν-type for N material. The I-region of a p-i-n diode can consist of either ν or π-type material. Figure 3.1(a) shows a P-ν-N diode structure. If the I-region is of sufficiently high resistivity, with few impurity atoms that will be ionized the depletion zone will extend throughout the I-region and include a small penetration into both the P and N-regions. Because of heavy doping in the P and N-regions the depletion zone will not extend very far into them, and the width of the depletion zone will be essentially equal to the I-layer width, W. Figure 3.1(b) shows the structure of P-π-N diode, the depletion zone width is approximately equal to the width of the intrinsic region. Most p-i-n diodes use ν material [Ref. 7: p. 41] for the I-layer.

B. THE ELECTRICAL EQUIVALENT CIRCUIT MODEL

The p-i-n diode used in microwave application has a simplified equivalent circuit under forward and reverse bias states as shown in Figure 3.2.

1. Forward Bias Equivalent Circuit

Under the forward bias state, both holes and electrons are injected into the I-region, and the mobile carriers form a conductive plasma whose resistivity depends on the carrier density obtained from the injection process. The forward bias resistance, R_f may be expressed as:

$$R_f = R_i + R_{sf} \qquad \text{(eqn 3.1)}$$

where R_i = resistance due to the I region, and

R_{sf} = resistance of P and N-regions and their ohmic contacts.

For an abrupt junction diode, the resistance due to the I-region can be expressed as follow:

$$R_i = \frac{W^2}{2\, i_f \mu_{av} \tau_L} \qquad \text{(eqn 3.2)}$$

where W = I-region thickness,

i_f = DC forward bias current,

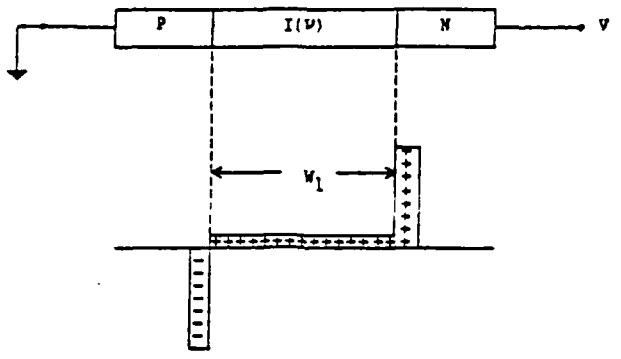
μ_{av} = the average carrier mobility, and

τ_L = the carrier lifetime in the intrinsic region.

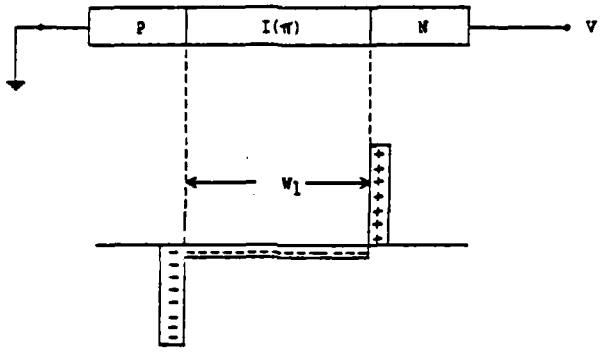
In the shunt configuration switching application the forward bias resistance, R_i, is the major factor of power dissipation in the diode. Since R_i is an inverse function of a DC bias current, i_f, we can increase i_f to minimize R_i. For low voltage p-i-n diodes, an i_f of 10 mA, and for high voltage p-i-n diodes 150 to 200 mA is sufficient to make R_f equal to R_{sf} [Ref. 9: p. 8].

2. Reverse Bias Equivalent Circuit

Under the reverse biased state, the I-region is depleted of carriers and the p-i-n diode appears as a constant capacitance to a microwave signal. The dissipation losses occur in the ohmic contacts and the resistances of the P and N-regions. R_r is used to represent these losses in the equivalent circuit model. Due to the capacitive reactance at microwave frequency, the circuit impedance of the p-i-n diode in its reverse bias

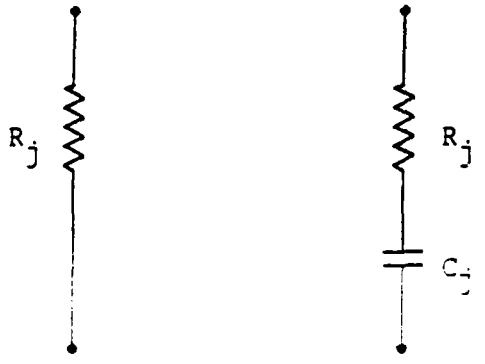


a. P-ν-N IMPURITY PROFILE



b. P-π-N IMPURITY PROFILE

Figure 3.1 Profiles for the two P-I-N Diodes Types.



FORWARD BIAS REVERSE BIAS

Figure 3.2 P-I-N Diode Chip Equivalent Circuit.

state is much larger than the impedance in the forward bias state. The capacitance, C_j of the p-i-n diode is determined by the diode size and I-region thickness as shown in equation 3.3

$$C_j \cong \frac{\varepsilon_0 \varepsilon_r \pi D^2}{4W} \qquad \text{(eqn 3.3)}$$

where ε_0 = free space permittivity,

ε_r = the relative dielectric constant of the material,

D = the junction diameter, and

W = I- region thickness.

This equation is valid for all reverse bias voltage magnitudes greater than the minimum voltage for complete I-layer depletion. Figure 3.3 shows equation 3.3 graphically for typical available p-i-n diode I-regions.

3. **P-I-N Diode Cutoff Frequency**

Hines [Ref. 4], defined a figure of merit for p-i-n diodes to relate the switching effectiveness in terms of switching cutoff frequency, f_{cs}. The Hines figure of merit is given by

$$f_{cs} = \frac{1}{2\pi C_j \sqrt{R_f R_r}} \qquad \text{(eqn 3.4)}$$

The figure of merit, f_{cs} is one of the parameters used in microwave switching design, and for $R_f = R_r$, f_{cs}/f is equal to the conventional diode Q. Knowing C_j, R_f, and R_r we can estimate the operating frequency range of the selected p-i-n diode from equation 3.4

C. POWER HANDLING

In the off-state of the microwave switch, the RF incident power is reflected back to the source or dissipated in the p-i-n diode. This dissipation causes the temperature of the junction to rise. For each diode there is a maximum temperature that it can withstand. The other factor which limits the amount of power handling is the peak voltage that appears across the junction, which can cause damage to the junction. In the p-i-n diode specification sheets these important parameters are available for the designer to estimate the power handling capability of the diode in the designed switches.

1. **Maximum Voltage across the P-I-N Diode**

The instantaneous voltage across a p-i-n diode junction is the algebraic sum of the RF voltage and DC bias voltage. If the junction voltage exceeds the device's breakdown voltage, the p-i-n diode is in the avalanche region, and the p-i-n diode acts as a low resistance causing high negative current flow and rapid temperature rise. Figure 3.4 shows the condition for a high RF voltage drive with reverse bias. The maximum voltage across the junction occurs when the diode is in the reverse bias state. The maximum instantaneous voltage applied to the junction is defined as:

$$V_{max} = V_{RF_{peak}} + V_{bias} \qquad \text{(eqn 3.5)}$$

where V_{bias} is the DC reverse bias impressed on the diode.

White [Ref. 7: p.155], suggested the conservative limit of the safe maximum voltage across the junction as:

$$V_{max} = 0.5\, V_b \qquad \text{(eqn 3.6)}$$

where V_b is the p-i-n diode breakdown voltage. A circuit designer may choose a different safety factor within an acceptable margin of safety for the designed switch.

2. **Maximum Junction Temperature**

The junction temperature of a p-i-n diode is determined by the ambient temperature of the circuit and the power dissipated in the diode. The dissipated power may be pulsed or CW. In either case, junction temperature must be kept below the maximum allowable value. This maximum temperature is dependent on the diode material (semiconductor), and the materials used in mounting and connecting to the semiconductor. The recommended maximum junction temperature for safe operation is 200°C [Ref. 10: p.290].

a. CW Power Dissipation

In the case of a continuous or a long-duration pulse, the temperature limit is determined by the initial temperature of the diode materials, the temperature of the heat sink, and thermal resistance between the wafer and the heat sink [Ref. 10: p.290]. θ_{jc} is the total thermal resistance unit in °C /watt. The junction temperature, T_j, for a given power dissipated, P_d, and the ambient temperature, T_a, is given by the equation:

$$T_j = T_a + P_d\theta_{jc} \qquad \text{(eqn 3.7)}$$

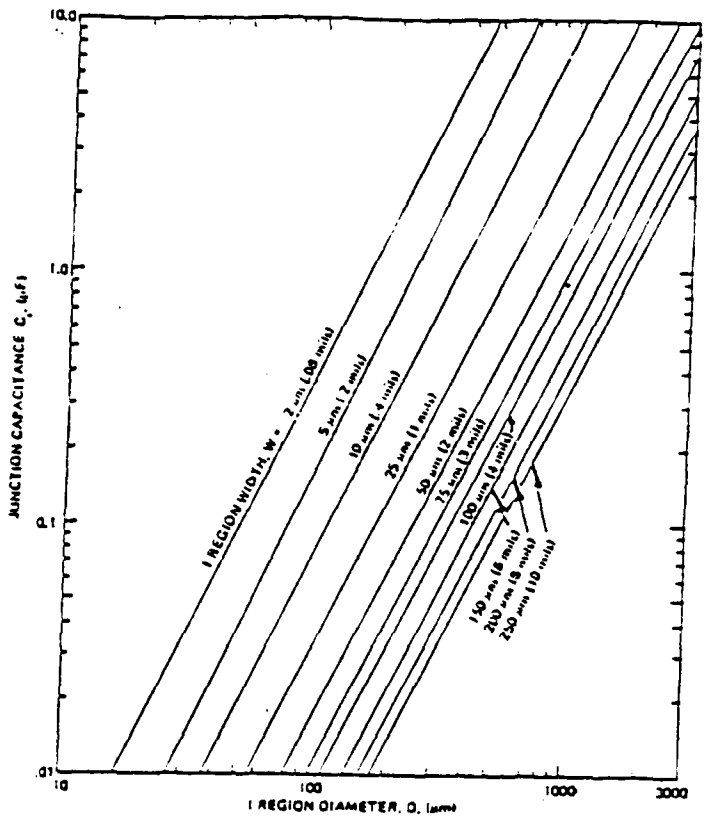


Figure 3.3 P-I-N Diode C_j vs. I-Region Diameter and Thickness.

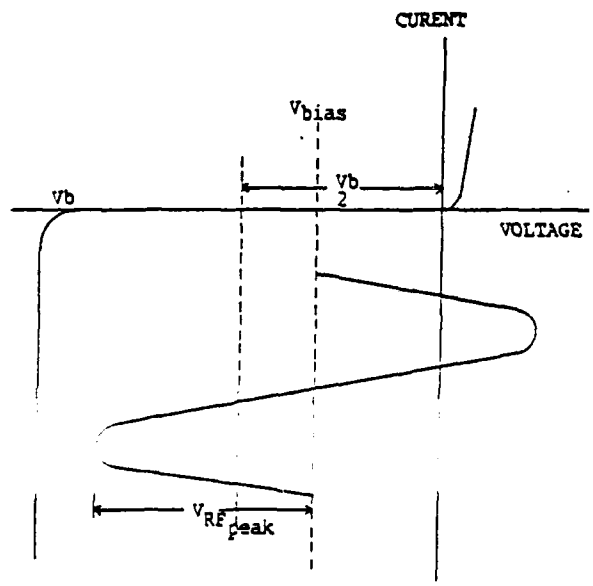


Figure 3.4 Junction Voltage at High RF and Reverse Bias.

The value of θ_{jc} is determined by the physical volume of the junction, material and geometry of the package. The maximum value of θ_{jc} for most glass packages can be as much as 600°C/watt. A large-area, high capacitance chip mounted on copper heat sink can have extremely low θ_{jc} of 5°C/watt or less [Ref. 9: p.10].

b. Pulse Power Dissipation

For a short duration pulse, the temperature limit is determined by the thermal time constant τ_{th} of the active region.

$$\tau_{th} = \theta_j HC \qquad \text{(eqn 3.8)}$$

where θ_j is the junction region thermal resistance, this value is available in the specification sheet or can be calculated from the diode physical size.

$$\theta_j = \frac{W}{K_{th}A} \qquad \text{(eqn 3.9)}$$

where W = the width of the I-region,

K_{th} = the thermal conductivity of the material,

A = the junction area, and

HC = the thermal capacity of the active region, also available in the specification sheet or can be calculated from:

$$HC = C_p \rho WA \qquad \text{(eqn 3.10)}$$

where C_p = the specific heat of the material, and

ρ = the density of the material.

For a pulse width of 0.25 τ_{th} or less, the pulse width is small compared with the thermal time constant. All the thermal energy is absorbed in the active region area, not spreading to the surrounding. The temperature rise of the junction, ΔT, in units of °C is expressed by:

$$\Delta T = \frac{P_d \Delta t}{HC} \qquad \text{(eqn 3.11)}$$

where Δt is the pulse duration. The junction temperature[6] T_j for a short pulse width from the above assumption is the sum of the ambient temperature and the temperature rise of the junction.

$$T_j = T_a + \Delta T \qquad \text{(eqn 3.12)}$$

For pulse widths of $0.50\tau_{th}$ to $3\tau_{th}$ the diode junction temperature follows an exponential curve given by the equation

$$T_j = T_a + P_d\,\theta j\,[1 - \exp(-t/\tau_{th})] \qquad \text{(eqn 3.13)}$$

Note that equation 3.13 contain θ_j, the junction thermal resistance and not θ_{jc} the total thermal resistance. For cooling between pulses, the junction temperature follows an exponential decay with the same time constant τ_{th} [Ref. 9: p.10].

D. TABLE OF TYPICALLY AVAILABLE P-I-N DIODES

To illustrate typical p-i-n diodes available for microwave switch design, Table 1 lists a number of typical diode chips from Microwave Associates, Inc. and their approximate electrical parameters. The symbols used in this table are already defined in this chapter.

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[6]Neglecting the heat flow from the junction.

TABLE 1
TYPICAL PARAMETERS OF P-I-N DIODES

MODEL NUMBER	MA-4P102	MA-4P103	MA-4P202	MA-4P203	MA-4P303	MA-4P404	MA-4P504
Minimum Vb(Volt)	50	30	100	100	200	300	500
Maximum Cj @ Vr(10) (pF)(Volt)	0.5	.15	.05	.15	.15	.20	.20
Maximum Rs @ If(10) (ohm)(ma)	2.5	1.5	2.0	1.5	1.5	0.6	0.6
Typical Carrier Lifetime(μS)	.100	.010	.100	.100	.200	1.00	2.00
Maximum Thermal Resistance (°C/watt)	60	40	60	30	30	20	20
Power (max) Dissipation at 25°C (watt)	2.5	3.75	2.5	5.0	5.0	7.5	7.5

IV. EVALUATION OF SEMICONDUCTOR MICROWAVE SWITCH CHARACTERISTICS

In this chapter, semiconductor device figures of merit, Kawakami's M and diode Q, are tested for the shunted switch configuration, to find the best parameter for use in a switch selection and/or design problem. From equation 1.5, we know that the figure of merit M, is a function of insertion loss, $S_{21}(1)$, in the switch on-state, and load isolation, $S_{21}(2)$, in the switch off-state. In order to solve the equation mentioned above, the switching characteristics, insertion loss and load isolation, should be provided. By using a CAD program (Touchstone) we can minimize the insertion loss in the switch on-state, and maximize the load isolation in its off-state. From the value of these two switching characteristics, we can compare and select the figure of merit that best characterizes the performance of this type of microwave switch. The power dissipation and heat removal requirements in the individual semiconductor device can be estimated from its terminal voltage. We will introduce two methods to evaluate the semiconductor device terminal voltage, and its power dissipation:

1. Using a Touchstone application program to evaluate the terminal voltage of interest.
2. Using a Fortran program written from the circuit model and method introduced in Chapter II.

A. INSERTION LOSS AND LOAD ISOLATION CALCULATION USING COMPUTER-AIDED CIRCUIT ANALYSIS PROGRAM (TOUCHSTONE)

The Touchstone program is advanced software for RF/microwave computer-aided engineering [Ref. 11]. It can provide an output of the S-parameters of a multi-port network and can perform an interactive optimization, and has applications which can be used in the measurement of selected terminal voltages. For a given electrical circuit, we can create a circuit file and evaluate circuit performance or use the optimization mode to get the optimized circuit-component values.

There are two alternative methods of approach to analyze these two switching characteristics. The first method uses semiconductor device parameters, diode junction resistance (R_j) and diode junction capacitance (C_j), as the direct input parameters of the circuit file. The second method employs semiconductor device figure of merit, diode Q, as an input parameter of the circuit file. In this approach the diode junction

capacitance and/or resistance are calculated in the circuit file, and then follow the same procedure as the first category.

Two types of microwave switches, single pole single throw, and single pole double throw switches, with one or multiple-semiconductor devices are investigated. By using the electrical equivalent circuit model introduced in Chapter II, we can create the circuit file following one of the above categories for the Touchstone system. The assumptions for the circuit model are:

1. All diodes in the switch are identical.
2. The transmission line configurations in the switch are symmetrical.[7]
3. The transmission line sections are lossless.
4. The transmission line impedance is between 30 to 90 Ohms.
5. The transmission line electrical length is between 30 to 120 degrees.

If the input of the circuit file is the figure of merit, or diode Q, then the junction resistance and junction capacitance are calculated from equations 4.2 and 4.3:

$$Q_{diode} = \frac{1000}{2\pi F_0 R_j C_j} \qquad \text{(eqn 4.1)}$$

$$R_j = \frac{1000}{2\pi F_0 C_j Q_{diode}} \qquad \text{(eqn 4.2)}$$

$$C_j = \frac{1000}{2\pi F_0 C_j Q_{diode}} \qquad \text{(eqn 4.3)}$$

where Q_{diode} is the figure of merit.

R_j is the diode junction resistance in ohm.

C_j is the diode junction capacitance in pF.

F_0 is the center frequency in GHz.

The relation of R_j, C_j and diode Q at the center frequency of 15 GHz. from equation 4.2, 4.3 is shown in Figure 4.1. In our circuit file for convenience we fix the value of capacitance and calculate the value of junction resistance (equation 4.2) and vary the value of diode Q.

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[7]For two-diode switches, TLIN1 is identical to TLIN3 (see Figures 4.3 and 4.7).

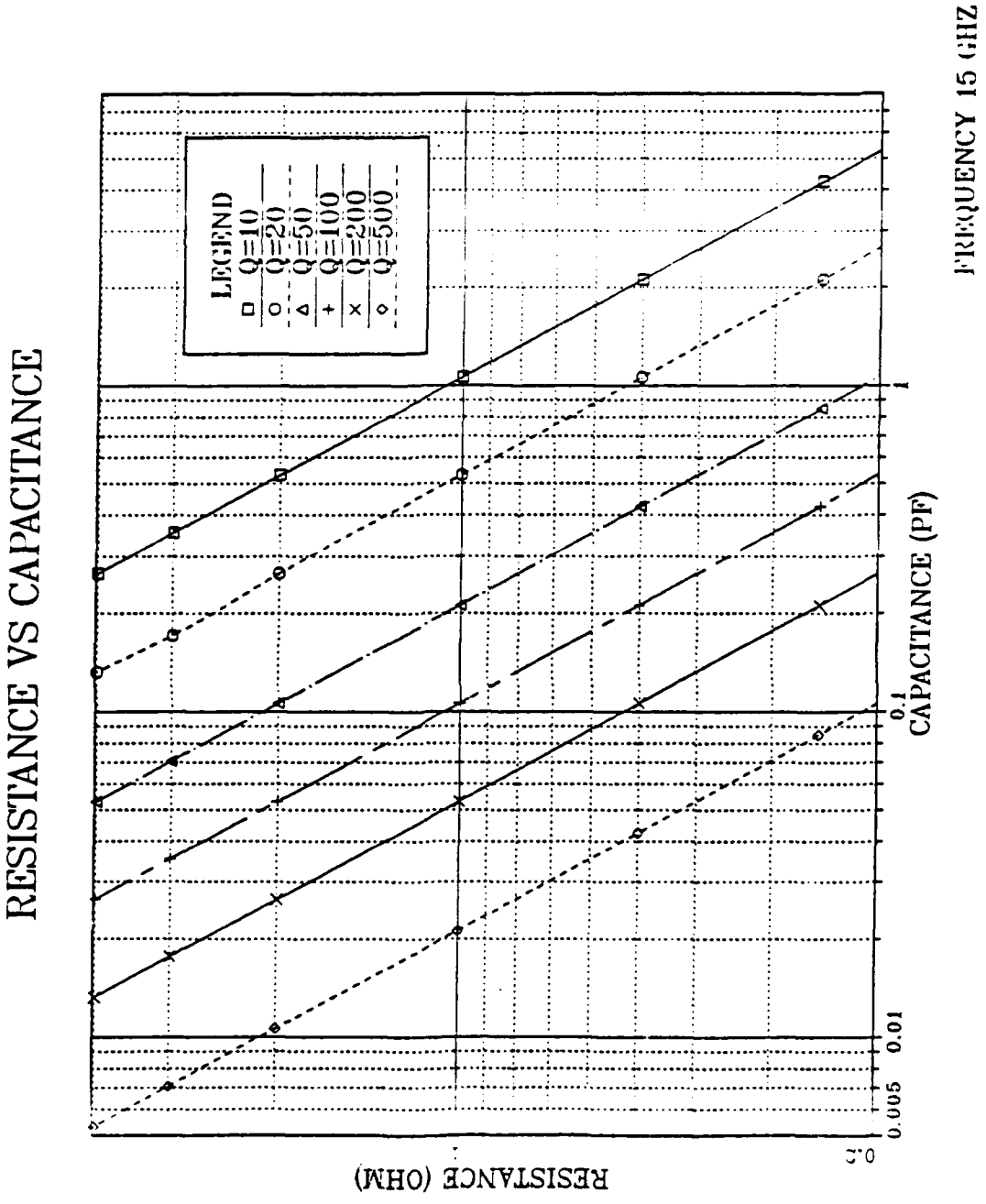

Figure 4.1 Resistance vs Capacitance as a Function of Diode Q.

In the procedure of creating a circuit file to optimize the switch characteristics for low insertion loss and high isolation, one more assumption is made; the impedance values of the diode are kept unchanged at the particular frequency in each state. The length and the characteristic impedance of the transmission line sections are varied to achieve the optimum switching characteristics in the operating frequency interval. In the optimization mode of the circuit file, we can minimize the switch insertion loss and maximize load isolation at the same time. This approach may require a long computation time to produce a result, and the switch insertion loss still may not approach the wanted value. It is found that a more efficient method of approach is to optimize only the insertion loss. The computation time is typically shorter, and normally produces satisfactory insertion loss and load isolation. Figure 4.2 is the flow chart of steps in creating a circuit file for the Touchstone system.

1. **Insertion Loss in the Switch On-state**

In the switch on-state, the ratio of the available power to the power reaching the load is defined as the insertion loss of the switch. In this switching state, the p-i-n diode is equivalent to a very high impedance in shunt with the circuit. A small amount of energy will be dissipated in the diode, but most of the energy is delivered to the load. Therefore the insertion loss of a well designed switch should be as low as possible. In order to achieve the low insertion loss, the optimization mode in the Touchstone system is used to perform the minimization of insertion loss to obtain the circuit design values. In practice the insertion loss has units of dB, and can be calculated from:

$$\text{Insertion loss in dB} = 10\log_{10}\frac{[P_{in}]}{[P_{load}]} \qquad \text{(eqn 4.4)}$$

From Chapter II, under the assumption of an ideal switch with matched load at both input and output ports, we can use the scattering matrices to represent the transmission behavior for both types of switches. Recall from Chapter II, for the on-state representation of S-matrices:

$$\text{SPST ON STATE: } [S] = \begin{bmatrix} 0 & 1 \\ 1 & 0 \end{bmatrix} \qquad \text{(eqn 4.5)}$$

$$\text{SPDT ARM (2) ON: } [S] = \begin{bmatrix} 0 & 1 & 0 \\ 1 & 0 & 0 \\ 0 & 0 & 0 \end{bmatrix} \qquad \text{(eqn 4.6)}$$

From equations 4.5 and 4.6, the insertion loss of the switch is defined as $|S_{21}|$ in dB[8] and can be evaluated from the circuit file of Touchstone system.

2. Load Isolation in the Switch Off-state

In the switch off-state, the load isolation of the switch is also defined by the ratio of the available power to the power reaching the load. In this switching state, the p-i-n diode is equivalent to a very low impedance in shunt with the circuit. Most of the energy is reflected back to the source, some of the energy is dissipated in the diode and a small amount of energy can transfer to the load. For an ideal switch in its off-state, the load isolation should be infinite, meaning that no energy is transferred to the load. In the real switch, the higher load isolation is the better switch performance. The load isolation has units of dB and has the same formula as in equation 4.4. In order to achieve the best performance of the designed switch, the Touchstone optimization mode is used, if desired, to optimize the load isolation as well as insertion loss. The S-matrix representation of the switch in the off-state with the same assumptions as for the insertion loss is defined as follows:

$$\text{SPST OFF STATE: } [S] = \begin{bmatrix} 1 & 0 \\ 0 & 1 \end{bmatrix} \qquad \text{(eqn 4.7)}$$

$$\text{SPDT ARM (3) ON: } [S] = \begin{bmatrix} 0 & 0 & 1 \\ 0 & 0 & 0 \\ 1 & 0 & 0 \end{bmatrix} \qquad \text{(eqn 4.8)}$$

From [Refs. 5,6], and equations 4.7 and 4.8 $|S_{21}|$ in dB is defined as the load isolation of the SPST switches, and S_{21} in dB is defined as the load isolation of the SPDT switches.

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[8]dB value = $20 \log_{10} S_{21}$

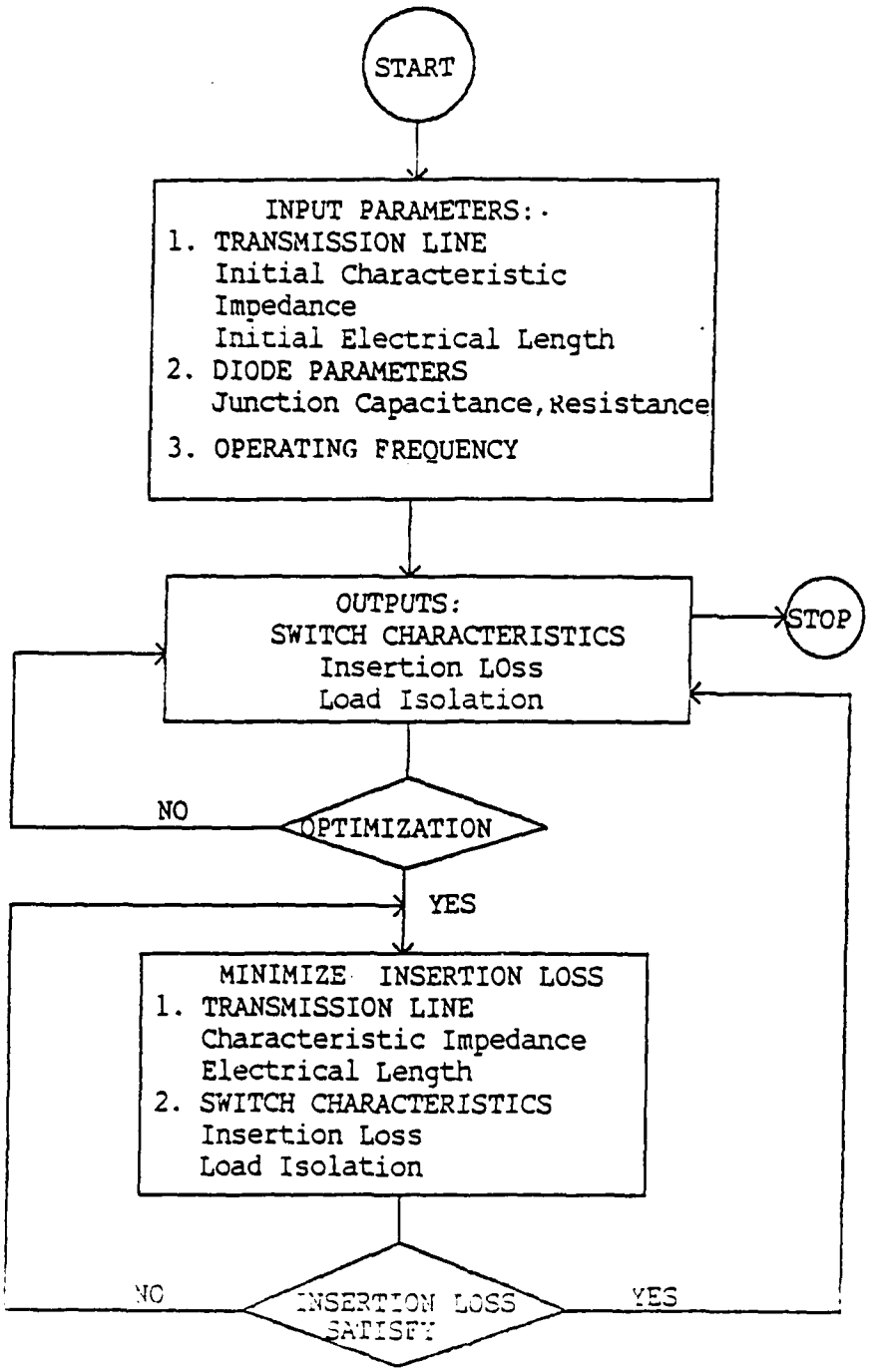

Figure 4.2 Flow Chart of a Circuit File.

3. Example of Insertion Loss and Load Isolation Evaluation

We divide the evaluation of switching characteristics into two cases:

1. Single pole single throw switch with two diodes.
2. Single pole double throw switch with four diodes.[9]

Two categories of creating the circuit file are applied to both cases.

a. SPST Two-Diode Switch

The electrical circuit representation of the SPST two-diode switch is shown in Figure 4.3(a). The switch on- and off-state equivalent circuits are shown in Figures 4.3 (b) and (c) respectively. To create a circuit file from the equivalent circuit, node numbers are assigned to every component, then the steps in Figure 4.2 are followed. The example of circuit files for switching characteristics, insertion loss and load isolation, evaluation of a SPST two-diode switch are listed in Appendix A.

SPSTD.CKT, listed in Appendix A1, is an example of the circuit file created for the single pole single throw switch in the first category, in which diode resistance and capacitance values are chosen and used as input data for the circuit file. Input parameters are diode junction resistance and diode junction capacitance from typical p-i-n diode parameters available in Table 1. We select the diode model number MA-4P203 with 0.15 pF junction capacitance and 1.5 ohms junction resistance to be the input parameters for the circuit file. After optimizing the circuit file from 10 to 20 GHz, we have the output file of the switch insertion loss and load isolation as shown in Table 2.

From the Touchstone output file listing in Table 2, LINDON and LINDOFF are switch insertion loss and load isolation respectively. Our required switch operating frequency range is between 10 and 20 GHz, the wanted value of switch insertion loss is around -0.1 to -0.2 dB and the load isolation greater than -45 dB. The characteristics of Table 2 satisfy our switch design requirement. The plot of insertion loss and load isolation is shown in Figure 4.4.

After optimization, the circuit-component values, characteristic impedances and electrical lengths of the transmission line sections, are given in the optimized circuit file. The optimized line-section parameters of the example in Appendix A1 are: transmission line section A has Z_a of 39.40 ohms and E_a of 106.3 degrees, transmission line section B has Z_a of 38.25 ohms and E_b of 62.7 degrees. In switch construction, to obtain the design value of the insertion loss and load isolation, the transmission line

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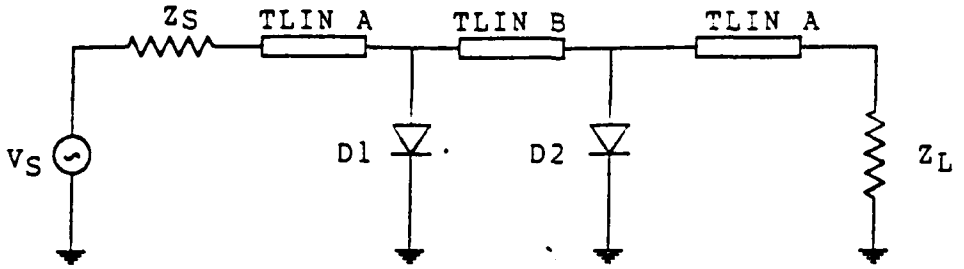
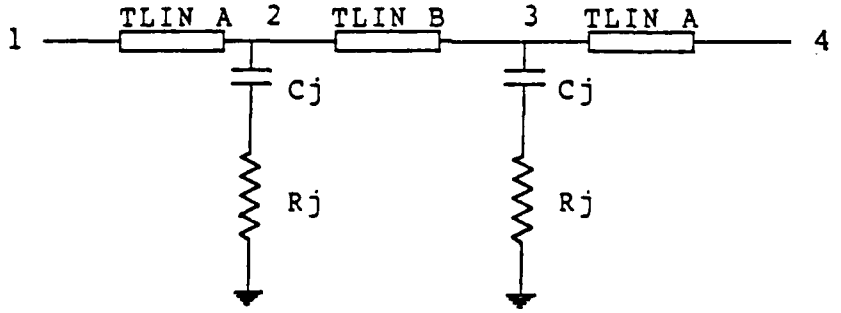
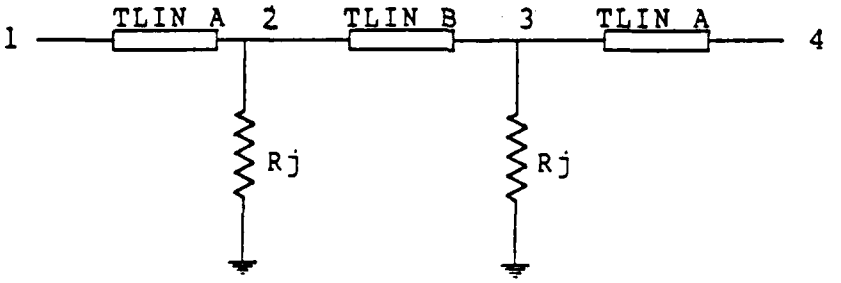
[9]There are two diodes in each branch of the switch.



4.3(a) SPST 2-DIODE EQUIVALENT CIRCUIT



4.3(b) SPST ON-STATE EQUIVALENT CIRCUIT



4.3(c) SPST OFF-STATE EQUIVALENT CIRCUIT

Figure 4.3 Single Pole Single Throw Switch Equivalent Circuit.

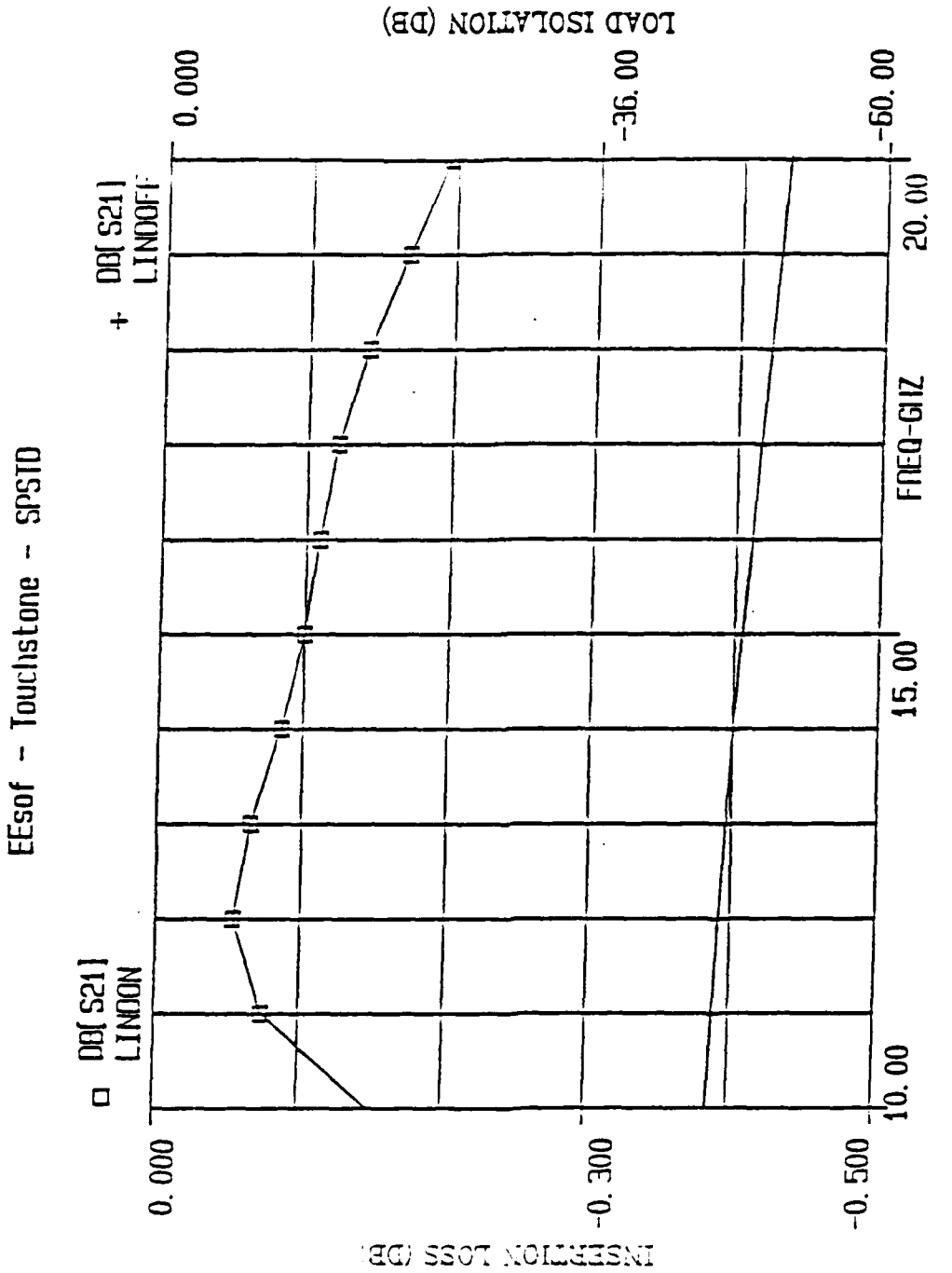


Figure 4.4 SPST Switch Insertion Loss and Isolation vs Frequency.

TABLE 2
TOUCHSTONE OUTPUT SPSTD.CKT

Frequency - GHz	dB [S21] LINDON	dB [S21] LINDOFF
10.0000	-0.150	-46.276
12.0000	-0.053	-47.025
14.0000	-0.085	-48.011
16.0000	-0.110	-49.261
18.0000	-0.141	-50.590
20.0000	-0.195	-51.750

sections in the switch should have their characteristic impedances and electrical lengths close to the calculated values.

SPSTQ.CKT, listed in Appendix A2, is an example of a circuit file created for the single pole single throw switch in which input parameters are Q_{diode} and diode junction capacitance. The selected value of junction capacitance is 0.15 pF and the value of diode Q are between 10 and 500 are used as input parameters of this circuit file. After optimizing the circuit file from 10 to 20 GHz we have the output file of the switch insertion loss and load isolation as shown in Table 3.

Table 3 is the collection of of SPSTQ.CKT outputs evaluated for different diode Q values. This table verifies that the diode Q has the character of a figure of merit, serving as an indicator of switching performance. The higher diode Q is, the better the switch characteristics: low insertion loss and high isolation.

Figures 4.5 and 4.6 show the plot of insertion loss vs frequency and load isolation vs frequency of a SPST switch with two diodes with diode Q as a parameter. We can use these two figures together with Figure 4.1 for a design problem of a SPST switch from a given specification. For example, a specification may require a two p-i-n diode SPST switch to have at least -0.1 dB insertion loss and isolation better than

TABLE 3
TOUCHSTONE OUTPUT SPSTQ.CKT

INSERTION LOSS IN dB

Frequency GHz	Diode Q = 10	Diode Q = 20	Diode Q = 50	Diode Q = 100	Diode Q = 200	Diode Q = 500
10.0000	-.367	-.342	-.135	-.064	-.056	-.052
12.0000	-.194	-.111	-.049	-.031	-.019	-.011
14.0000	-.342	-.170	-.082	-.062	-.044	-.034
16.0000	-.499	-.231	-.101	-.052	-.037	-.013
18.0000	-.517	-.269	-.134	-.072	-.039	-.019
20.0000	-.724	-.393	-.186	-.096	-.048	-.019

LOAD ISOLATION IN dB

Frequency GHz	Diode Q = 10	Diode Q = 20	Diode Q = 50	Diode Q = 100	Diode Q = 200	Diode Q = 500
10.0000	-20.21	-30.53	-47.38	-58.78	-70.62	-86.42
12.0000	-20.51	-30.84	-48.06	-59.46	-71.30	-87.09
14.0000	-21.05	-31.37	-48.88	-60.53	-72.37	-88.17
16.0000	-21.89	-32.27	-50.17	-61.90	-73.76	-89.57
18.0000	-22.93	-33.42	-51.39	-63.26	-75.14	-90.96
20.0000	-23.95	-34.57	-52.40	-64.28	-76.18	-92.01

-60.00 dB at the mid-frequency of 15 GHz. In Figure 4.5, with the value of diode Q 50 or more the switch can have insertion loss less than -0.1 dB. But from Figure 4.6 the diode Q of 50 is not great enough to obtain load isolation of -60.00 dB.

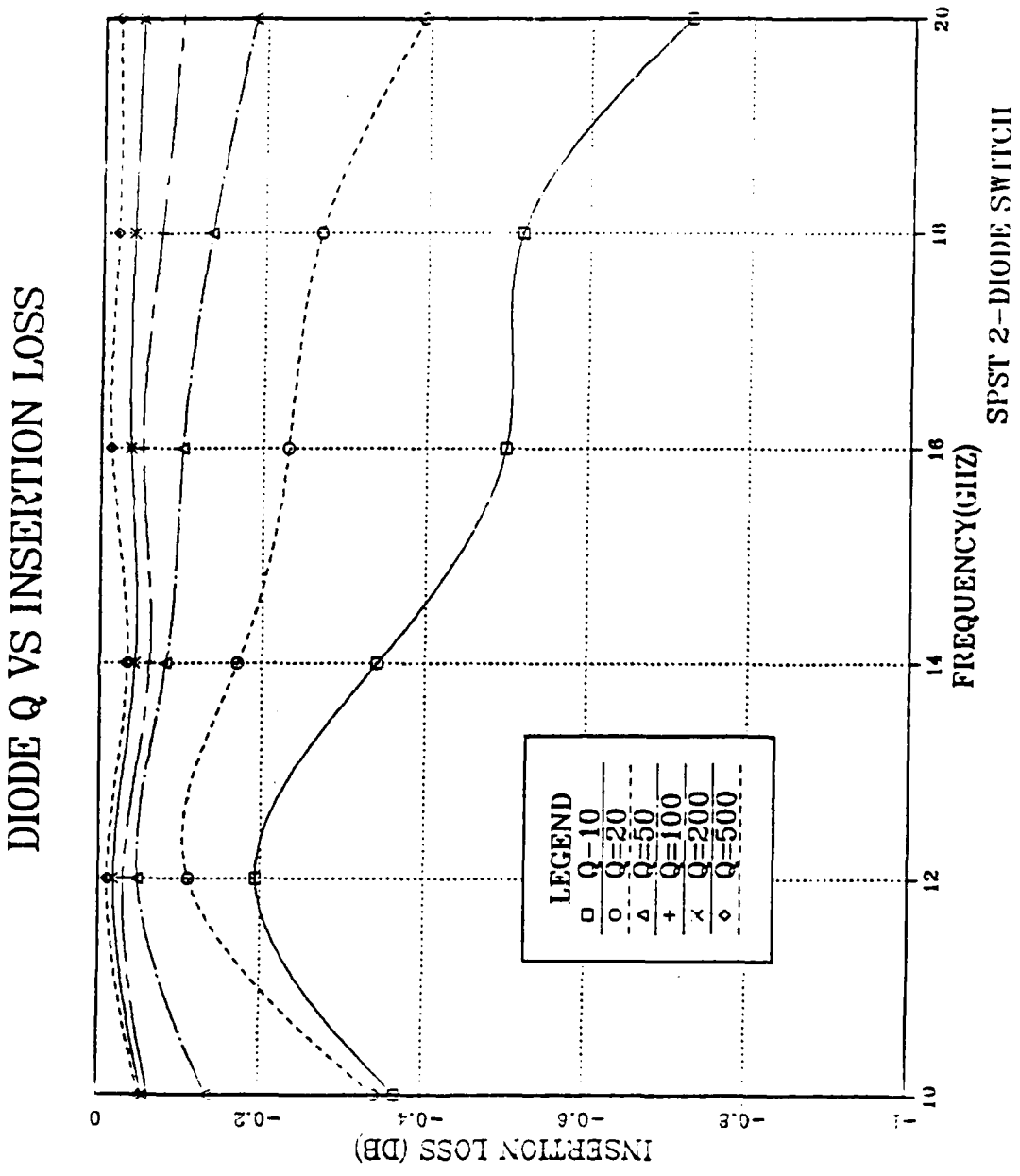


Figure 4.5 SPST Switch Insertion Loss vs Q_{diode}

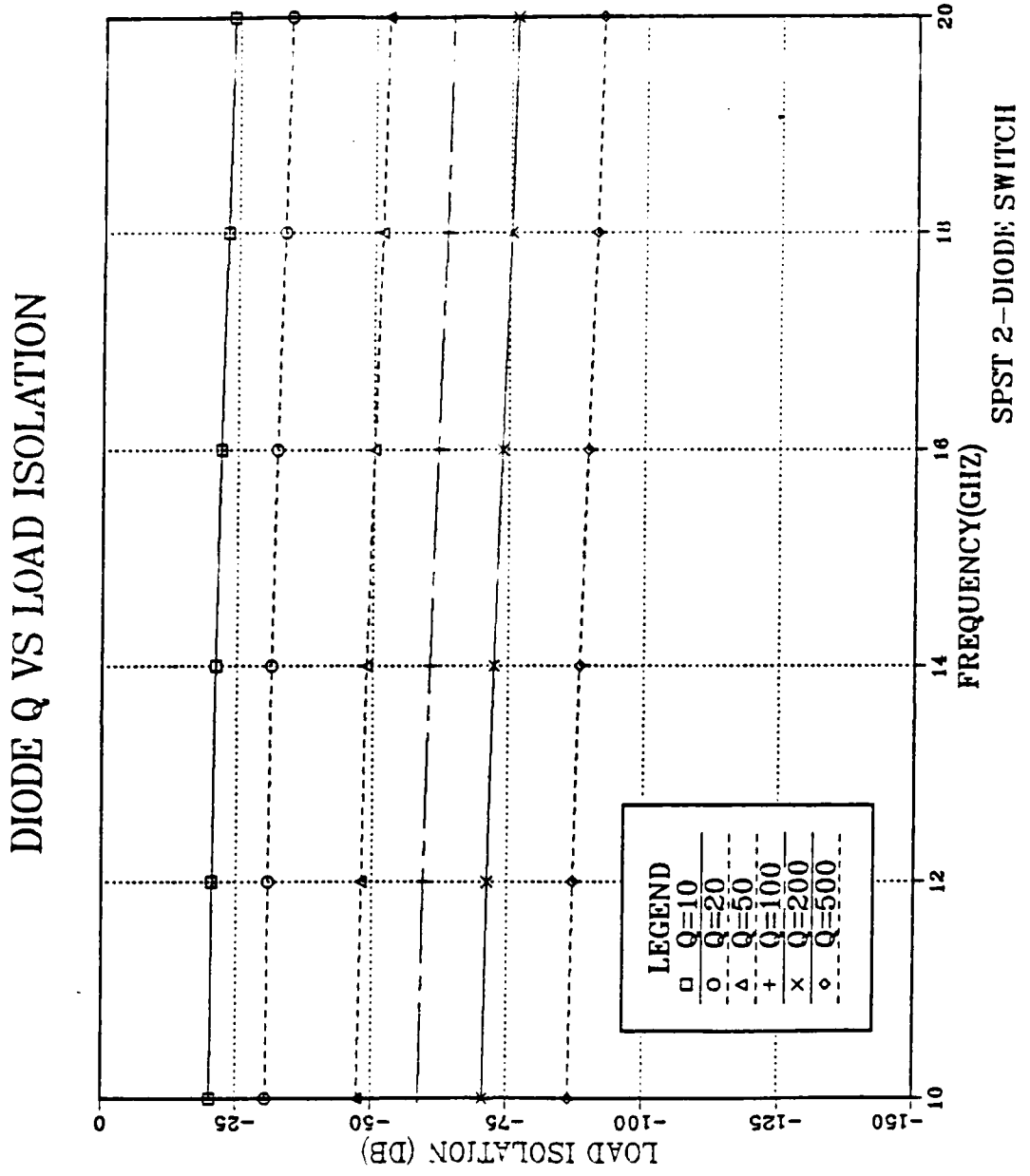


Figure 4.6 SPST Switch Load Isolation vs Q_{diode}

Therefore we select a diode for the switch that has the value of Q_{diode} of 100. From Figure 4.1 with the Q = 100 curve we can choose one of the p-i-n diodes that has the value of junction capacitance and resistance close to our estimated value. If we select p-i-n diode model number MA-4P504 with diode junction capacitance of 0.2 pF and junction resistance of 0.6 ohm, at 15 GHz we obtain the diode Q value of 88.42, switch insertion loss of -.102 dB and isolation of -60 dB from the modified SPST.CKT circuit file.

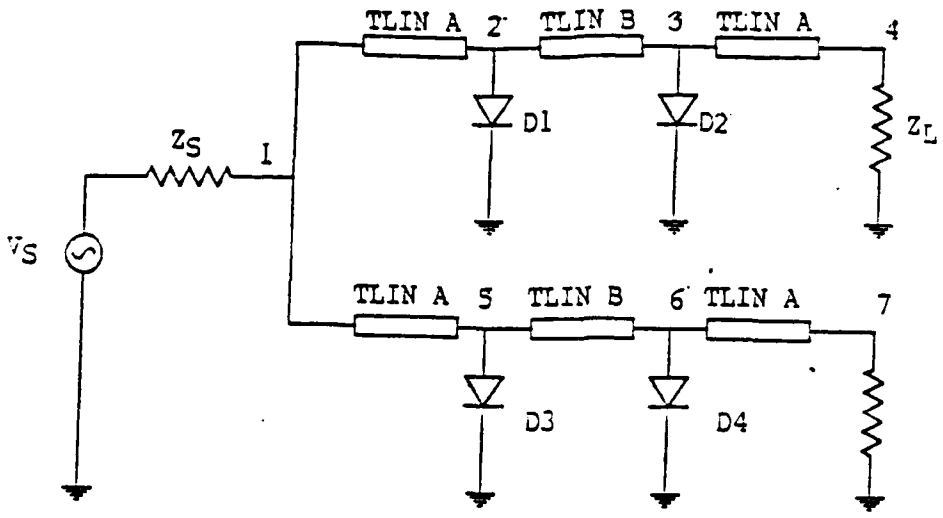
b. SPDT Four-Diode Switch

A single pole double throw switch is considered as two SPST.switches with input arms tied together, when one arm is in the on-state, the other is in the off-state. A SPDT four-diode switch has the electrical circuit representation and the switch on off-state equivalent circuit shown in Figure 4.7(a) and (b) respectively. To create a circuit file from the equivalent circuit, the same procedure can be followed as in SPST switch case. Or we can make some necessary modifications to the SPST switch circuit files in Appendix A. The example of circuit files for evaluating SPDT switch insertion loss and load isolation are listed in Appendix B.

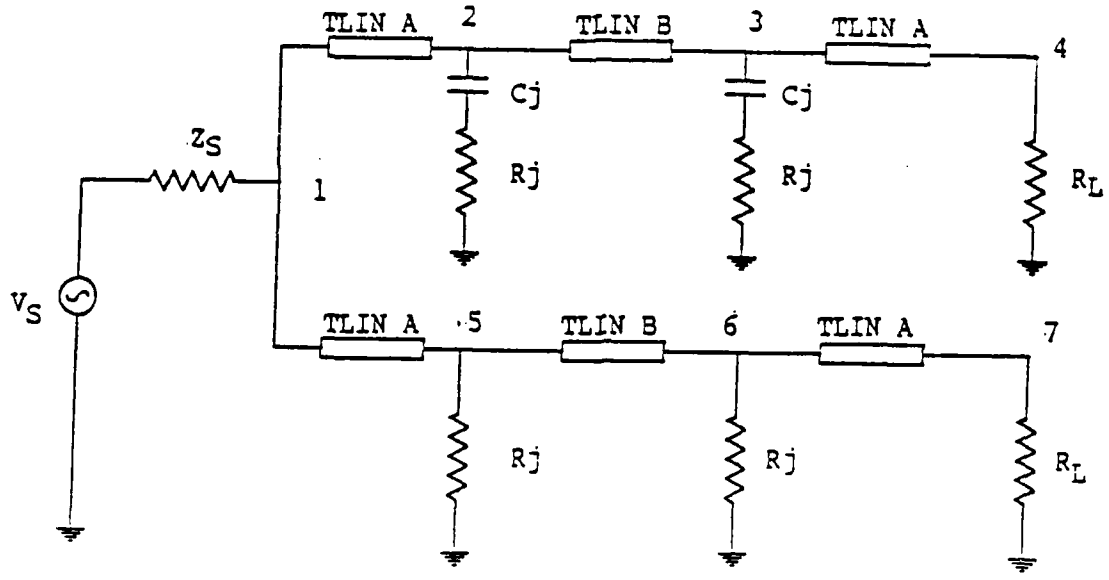
SPDTD.CKT, listed in Appendix B1, is an example of the circuit file used for the single pole double throw switch with four diodes. With the same p-i-n diode model number as in the circuit file SPSTD.CKT, after optimizing this circuit file from 10 to 20 GHz, we have the output file of the insertion loss and load isolation shown in Table 4. The optimized transmission line section characteristic impedances and electrical lengths are: 46.56 ohms and 93.58 degrees for transmission line section A, 89.06 ohms and 32.82 degrees for transmission line section B.

The output file listing in Table 4 shows that for the required operating frequency between 10 to 20 GHz, the designed SPDT four-diode switch using p-i-n diode model number MA-4P203 with 0.15 pF junction capacitance and 1.5 ohms junction resistance, has insertion loss around -1.0 dB and load isolation greater than -50 dB We realize that the insertion loss of the SPDT switch case is not so low as for the SPST switch case. However the insertion loss and load isolation satisfy the general requirement of a switch design problem. The plot of insertion loss and load isolation vs operating frequency is shown in Figure 4.8.

SPDTQ.CKT, listed in Appendix B2, is an example of the circuit file created for the single pole double throw switch for which input parameters are Q_{diode} and diode junction capacitance. In this example, the value of 0.15 pF junction



4.7(a) SPDT 4-DIODE SWITCH EQUIVALENT CIRCUIT



4.7(b) SPDT ON,OFF-STATYE EQUIVALENT CIRCUIT

Figure 4.7 Single Pole Double Throw Switch Equivalent Circuit.

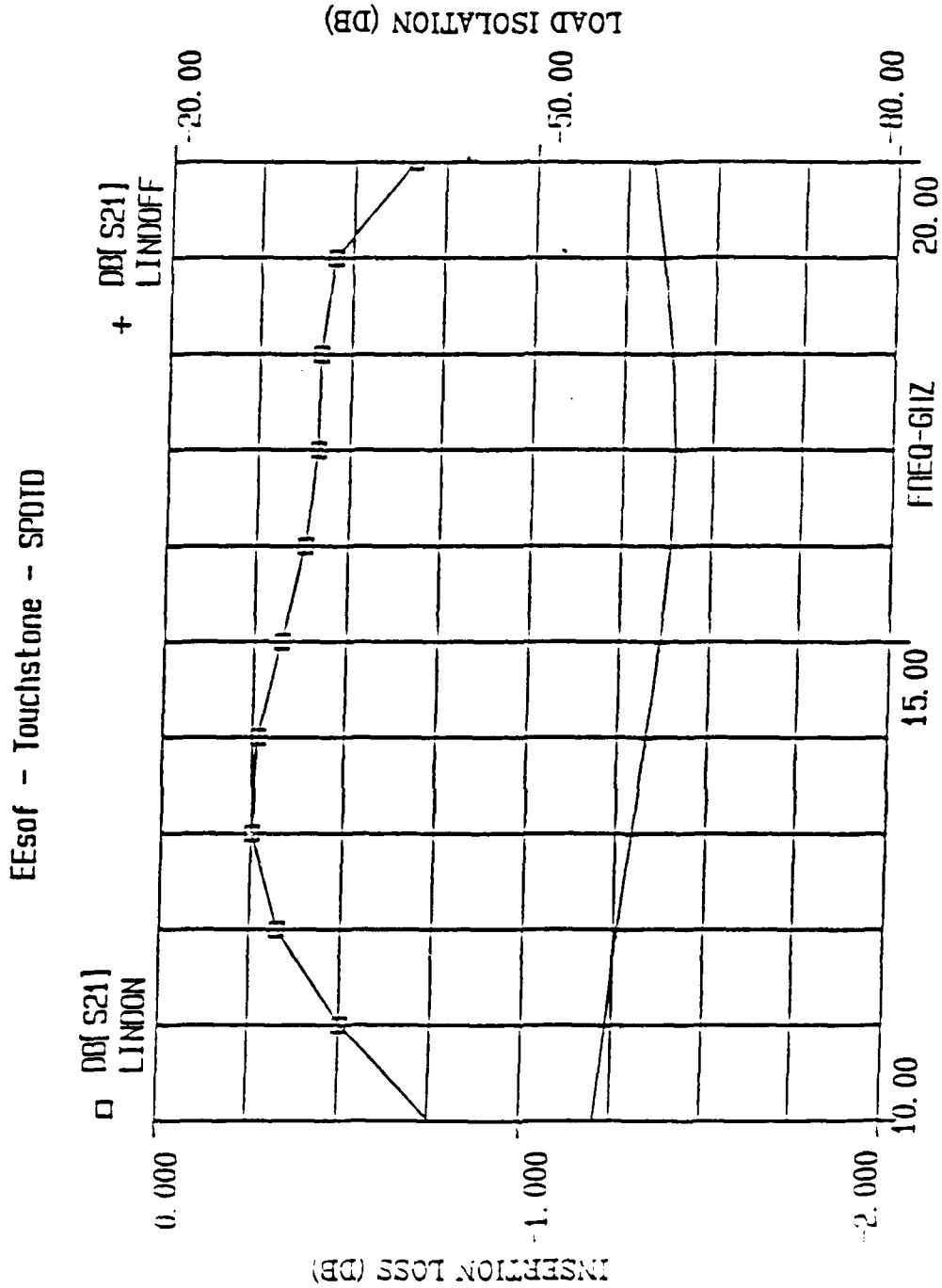


Figure 4.8 SPDT Switch Insertion Loss and Isolation vs Frequency.

TABLE 4
TOUCHSTONE OUTPUT SPDTD.CKT

Frequency - GHz	dB [S21] LINDON	dB [S21] LINDOFF
10.0000	-0.756	-56.199
12.0000	-0.327	-57.856
14.0000	-0.226	-59.898
16.0000	-0.385	-61.603
18.0000	-0.417	-61.471
20.0000	-0.665	-59.573

capacitance, and values of diode Q from 10 to 500 are selected and used as input parameters of the circuit file. The optimized output file SPDTQ.CKT is shown in Table 5.

For general use of diode Q as the figure of merit to characterize the switching performance of this type of switch, the choice of junction capacitance value selected as input parameter to the Touchstone file does not strongly affect the Q-dependence of switch performance shown in Table 5. The result of output file SPDTQ.CKT listed in Table 5 verifies that the diode Q has the character of a figure of merit, serving as an indicator of the switch performance. In a switch design problem, diode Q can be used as a parameter that characterizes the switching transmission characteristics. The plot of insertion loss and load isolation vs operating frequency as a function of diode Q from the results in Table 5 are shown in Figures 4.9 and 4.10. These two plots can be used in a design problem of a SPDT switch from a given specification. The procedures for the design of a SPDT switch are the same as mentioned in the SPST switch case.

TABLE 5
TOUCHSTONE OUTPUT SPDTQ.CKT

INSERTION LOSS IN dB

Frequency GHz	Diode Q = 10	Diode Q = 20	Diode Q = 50	Diode Q = 100	Diode Q = 200	Diode Q = 500
10.0000	-1.96	-1.38	-1.04	-.926	-.824	-.796
12.0000	-1.36	-.725	-.345	-.217	-.148	-.117
14.0000	-1.13	-.577	-.265	-.179	-.129	-.095
16.0000	-1.32	-.756	-.394	-.294	-.232	-.190
18.0000	-1.69	-.935	-.395	-.214	-.118	-.059
20.0000	-2.37	-1.49	-.835	-.564	-.515	-.425

LOAD ISOLATION IN dB

Frequency GHz	Diode Q = 10	Diode Q = 20	Diode Q = 50	Diode Q = 100	Diode Q = 200	Diode Q = 500
10.0000	-33.55	-44.74	-59.50	-71.18	-83.59	-99.46
12.0000	-34.35	-45.92	-60.83	-72.58	-85.09	-100.95
14.0000	-35.82	-47.90	-63.08	-74.99	-87.56	-103.43
16.0000	-37.56	-49.71	-64.75	-76.66	-89.13	-105.00
18.0000	-38.27	-49.68	-64.27	-75.97	-88.18	-105.04
20.0000	-37.54	-48.24	-62.75	-74.37	-86.21	-102.20

B. THE SEMICONDUCTOR DEVICE FIGURE OF MERIT WHICH BEST CHARACTERIZES THE SWITCHING PERFORMANCE

Two well known figures of merit were used as parameters to predict the switching performance of semiconductor microwave switches. In this thesis research, the

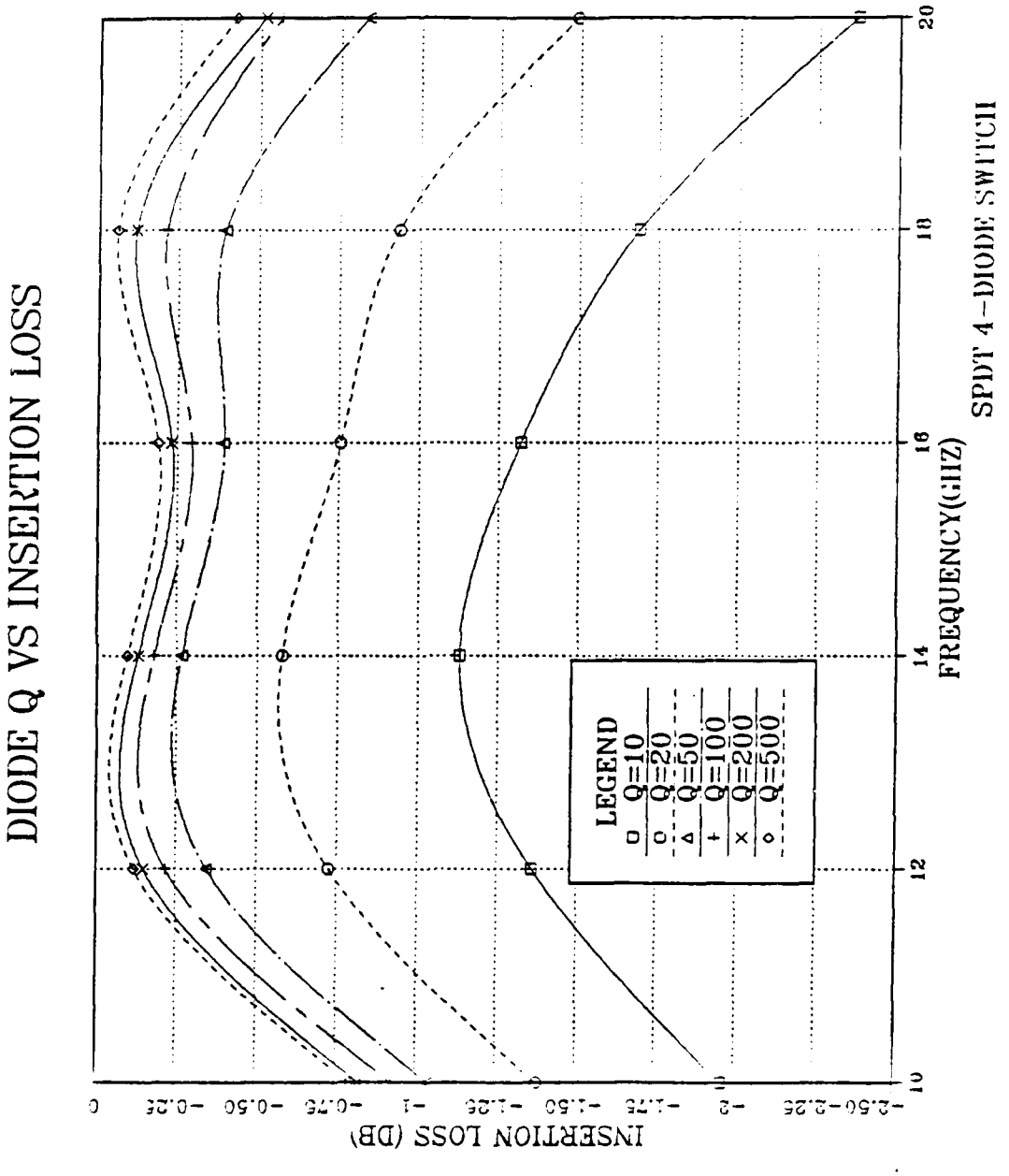


Figure 4.9 SPDT Switch Insertion Loss vs Q_{diode}

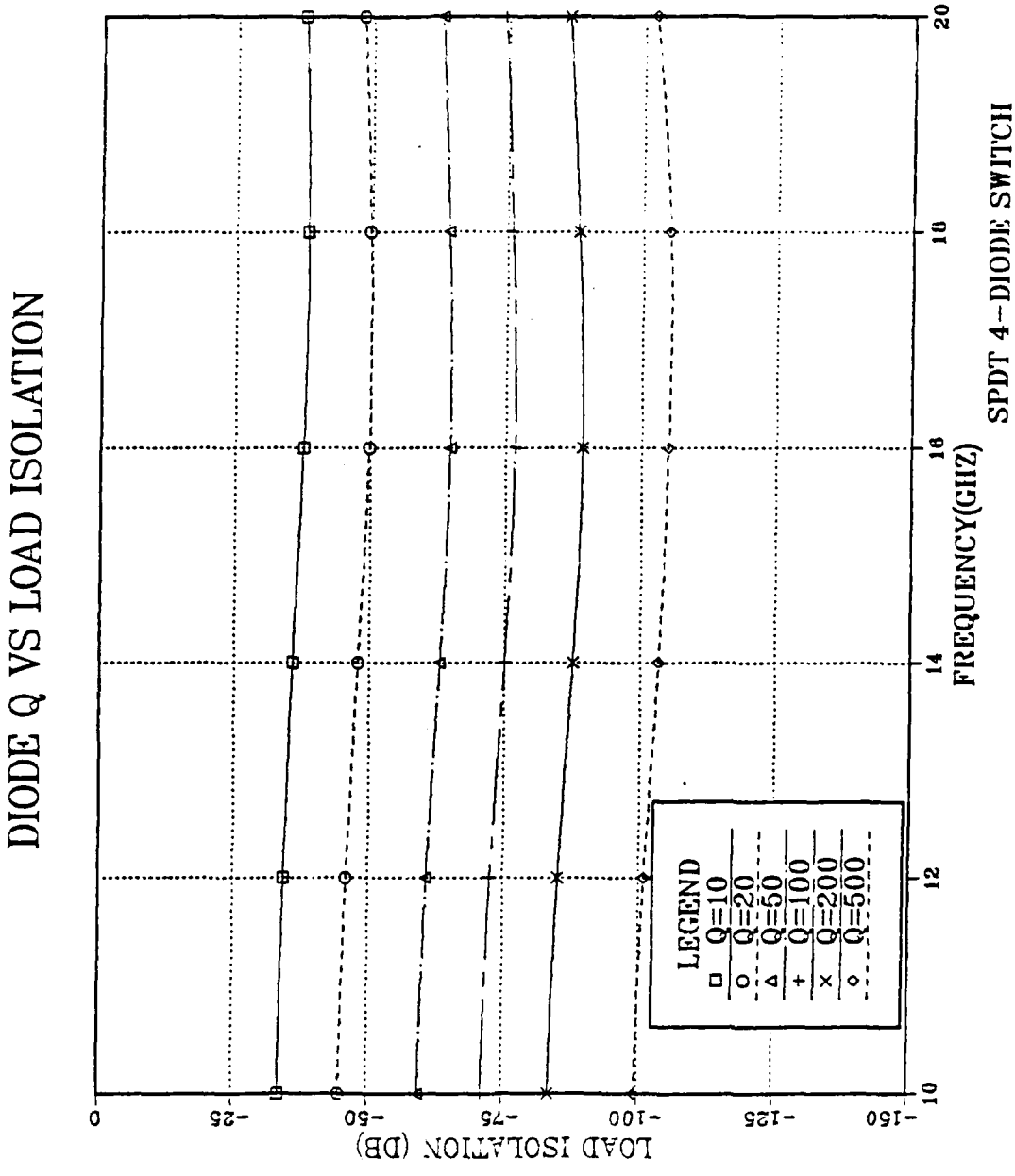


Figure 4.10 SPDT Switch Load Isolation vs Q_{diode}

semiconductor device considered is the p-i-n diode, used in a shunt-configuration microwave switch. The conventional diode Q was shown to coincide with the simplified equation of Kurokawa and Schlosser for quality factor Q, and therefore we use the conventional Q as our semiconductor device figure of merit. In Chapter II equations 2.10 and 2.11 showed the relationship between both figures of merit: the diode Q and Kawakami's M. To verify these two equations, we investigated the relationship of Kawakami's M and the switch transmission characteristics defined in equation 1.5. Optimal values of switch insertion loss and load isolation were evaluated from the Touchstone circuit file which has the diode Q as an input parameter. For the SPDT switch case, values of insertion loss and load isolation evaluated with different diode Q values at 15 GHz. are substituted in equation 1.5, and the results are listed in Table 6.

TABLE 6
COMPARISON BETWEEN FIGURES OF MERIT M, AND DIODE Q

Diode Q	S_{21} (1)	S_{21} (2)	M (eqn 1.5)	$\frac{\Delta M}{\Delta Q} \times 100$ (%)
10.0000	0.9421413	0.1590319	0.9770399	
				0.1667
20.0000	0.9677804	0.0865225	0.9937131	
				0.0161
50.0000	0.9830945	0.0404859	0.9985498	
				1.8e-3
100.000	0.9872322	0.0222759	0.9994510	
				2.9e-4
200.000	0.9897033	0.0118343	0.9997507	
				[illegible]
500.000	0.9915362	0.0053798	[illegible]	

Table 6 shows the comparison of the two figures of merit, with M calculated from equation 1.5. Note that in this table $S_{21}(1)$, $S_{21}(2)$ correspond to switch

insertion loss and load isolation respectively, where the value of S_{21} is in the form: $S_{21} = 10^{(db/20)}$. The values of M are less than 1 as mentioned earlier. For this type of switch at Q_{diode} of 10 the value of M is 0.9762, and at Q_{diode} of 500 the value of M is 0.9999. For typical diode Q values, M departs very little from unity, and the percentage of deviation is reduced tremendously in the high Q region. Thus the parameter Q_{diode} is more convenient to use due to its wider range compared with the parameter M. When tested for different types of switch,[10] the results are nearly the same as shown in Table 6 for all the values of M (almost unity and small deviation in each interval). An additional reason in support of our decision to select the conventional diode Q as the best figure of merit to characterize switching performance is that it is well known and widely used. Table 7 shows the comparison of the result from Table 6 and values of M calculated from equations 2.10 and 2.11, this table verifies that equation 2.10 can be used to convert the diode Q value to the figure of merit M, and vice versa.

TABLE 7

COMPARISON OF FIGURES OF MERIT M, FROM DIFFERENT APPROACHES

Diode Q	M (eqn 1.5)	M (eqn 2.10)	M (eqn 2.11)
10.0000	0.9770399	0.9805806	0.9800000
20.0000	0.9937131	0.9950372	0.9950000
50.0000	0.9985498	0.9992001	0.9992000
100.0000	0.9994108	0.9998000	0.9998000
200.0000	0.9997507	0.9999499	0.9999500
500.0000	0.9999076	0.9999919	0.9999920

[10]SPDT switch with tuning stub, microstrip model.

C. NODAL VOLTAGE CALCULATION USING TOUCHSTONE PROGRAM

The power dissipation in a particular diode can be calculated by the voltage across its resistance or the current flow in the resistor of the p-i-n diode equivalent circuit. In the Touchstone program there is a technique for probing the nodes within a circuit file to determine the voltages at those nodes. An ideal voltage-controlled voltage source (VCVS) is used as a non-loading voltmeter probe [Ref. 12]. The input terminals of the VCVS are connected to the nodes between which the voltage is to be determined. The output terminals are connected to an output port so that the voltages may be read. The voltages read out from this method are normalized to unity value of the open circuit generator voltage [Ref. 12]. Appendix C shows examples of the Touchstone circuit files written for the evaluation of nodal voltages of SPST and SPDT switches. For SPDT switch case, the equivalent circuit model using in nodal voltage calculation is shown in Figure 4.11.

The circuit file SPDTV.CKT, listed in Appendix C2, is an example of a Touchstone circuit file using VCVS modules acting as voltage probes reading the nodal voltages from the attached terminals. The input parameters for this circuit file are the diode parameters and the optimal transmission line section values of the SPDT switch evaluated in Appendix B2. The major disadvantage of the Touchstone circuit file is that we can define up to four ports in our circuit file, meaning that we can measure no more than three nodes at a time. To measure a SPDT switch with four diodes, there are six nodes of interest. The first three nodes are measured in the SPDTV.CKT circuit file, while the last three nodes are measured by making some modifications to this circuit file (by moving the VCVS module to the new positions). The output files of SPDTV.CKT are listed in Table 8.

Knowing terminal voltage across the resistive part of the p-i-n diode equivalent circuit both on and off-state, the next step is to calculate the power dissipation in the individual p-i-n diode from the equation:

$$P_n = \frac{V_n^2}{R_n} \qquad \text{(eqn 4.9)}$$

where P_n is the dissipated power at node n,

V_n is the terminal voltage at node n, and

R_n is the resistive component of the n^{th} p-i-n diode.

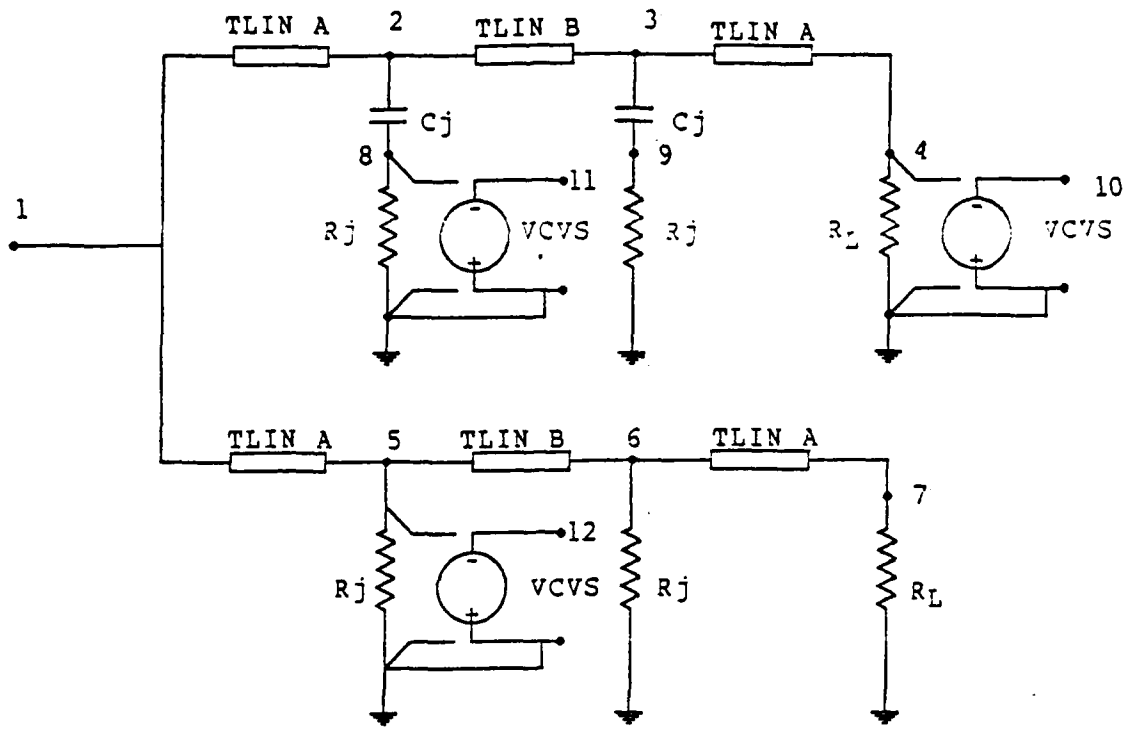


Figure 4.11 Nodal Voltage Measurement Equivalent Circuit.

TABLE 8
NODAL VOLTAGE FROM TOUCHSTONE SPDTV.CKT

	SWITCH ON-STATE			SWITCH OFF-STATE		
Frequency	V_{load}	V_{D1}	V_{D2}	V_{load}	V_{D1}	V_{D2}
10.0000	.458	.006	.006	7.7e-4	.017	7.3e-4
12.0000	.482	.008	.008	6.4e-4	.016	6.0e-4
14.0000	.485	.010	.009	5.1e-4	.015	4.7e-4
16.0000	.478	.012	.010	4.2e-4	.014	3.9e-4
18.0000	.477	.015	.011	4.2e-4	.015	4.0e-4
20.0000	.463	.018	.012	5.3e-4	.021	5.0e-4

In practice the dissipated power in a particular diode is normalized to the power delivered to the load in the switch on-state. Therefore each power dissipation calculated from equation 4.9 is normalized to the switch on-state output power. For the normalized power value, equation 4.9 becomes:

$$P_n = \frac{[V_n]^2 R_{load}}{[V_{load}]^2 R_n} \qquad \text{(eqn 4.10)}$$

where V_{load} is the load terminal voltage of the switch on-state.

The use of Touchstone circuit files, SPSTV.CKT and SPDTV.CKT, is very convenient for evaluating the diode terminal voltage, but we cannot use Touchstone to solve for power dissipation and the diode junction temperature problem directly. To do so one may use a hand calculator or write a special computer program calculating the power dissipation in each diode from equation 4.10, and use these dissipated powers to calculate the heat production from equations in Chapter III. However we see that the Touchstone output file has only three significant digits after the decimal point, meaning that numerical round off takes place in the third digit. These outputs generally satisfy engineering requirements. However for a very small nodal voltage across the diode, these rounded off outputs may cause significant error when we substitute them in a quadratic equation such as equation 4.10. It is a serious disadvantage to use these outputs for high output power microwave switches. For example an output voltage of 0.010 from Touchstone to represent a value of 0.0103 volts can cause an error of 0.88 watts of diode power in a one kilowatt switch. This number may look small, however it can cause an error of 30-40°C in diode junction temperature rise. This error can affect the decision of selection of a proper p-i-n diode for the switch design.

D. EVALUATION OF POWER DISSIPATION AND HEATING USING FORTRAN PROGRAM

To avoid some disadvantages of the use of the Touchstone nodal voltage evaluation for power computation, we may search for another CAD program or create a specific computer program to solve this problem. Many microwave CAD programs have been written in FORTRAN IV for both mainframe and minicomputers, but up to now there is no program written to solve for the power dissipation in a microwave circuit [Ref. 7]. The Fortran language requires specific formats of input and output

and has to be compiled before running the program. Nonetheless, the advantages to the microwave engineer are its complex number notation, and double precision capability. These two advantages lead to accurate outputs, for example in the multiplication of more than ten complex matrices in cascade. To write a Fortran program to evaluate the terminal voltages of the diode microwave switch equivalent circuit, electrical two-port components of the switch are converted into simple appropriate two-port matrix forms. In chapter 2 we introduced an ABCD matrix representation of the two-port networks for a transmission line section, a shunt admittance and series impedance in the lumped-circuits. For our switch circuit model, the circuit components are characterized as boxes in cascade connecting with the applied voltage at one end and the load at the other end.

To evaluate the power dissipation and junction temperature in the diodes of a SPDT switch which has an equivalent circuit shown in Figure 4.12, with the optimal transmission line sections by use of Touchstone, the procedure follows the flow diagram shown in Figure 4.13.

1. **Nodal Voltage and Current Calculation**

We assume that the switch is supplied by a one volt generator with 50 ohms series impedance. First we divide the equivalent circuit into two parts, one the on-state branch the other the off-state branch. For both on- and off-states, each transmission line section and the diode equivalent circuit two-port network is transformed into ABCD matrix form (Figure 4.12(a)) by subroutine MATRIX. This subroutine using equations 2.18 and 2.19 for the transformation of a shunt diode and a lossless transmission line section into ABCD two-port matrices respectively. To obtain the voltages and currents in the circuit, the successive input impedances of the individual two-port elements must be determined. All two-port networks in the branch are cascaded by subroutine MATMUL and produce a new equivalent circuit as in Figure 4.12(a). Subroutine MATMUL provides a complex matrix product of a pair of matrices. From Figure 4.12(b), input impedance in each branch (Z_{inon}, Z_{inoff}) is calculated from equation 2.21. The impedance of the switch (Z_{in}) is determined by the paralleling of input impedances of both branches (Z_{inon} Z_{inoff}). The switch input current (I_{in}) and input voltage (v_{in}) from the generator are calculated from equations 2.22 and 2.23. The next step is to find the currents and voltages in the on- and off-state branches. The input voltage on each branch is equal to the switch input voltage (paralleled ports). Current flow in the on- and off-state branches is determined by current divider method as follows:

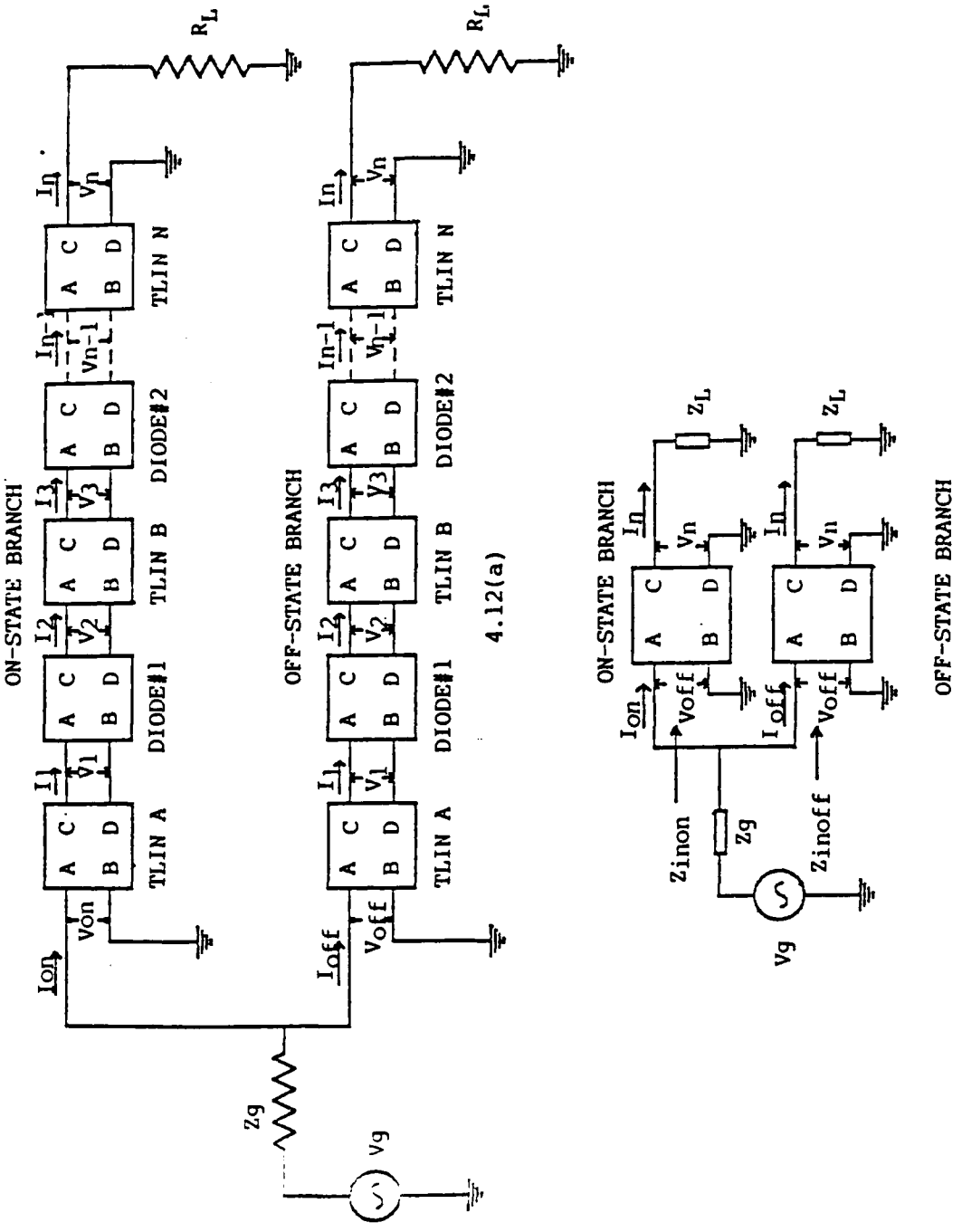


Figure 4.12 ABCD Matrix Representation of SPDT switch Circuit Model.

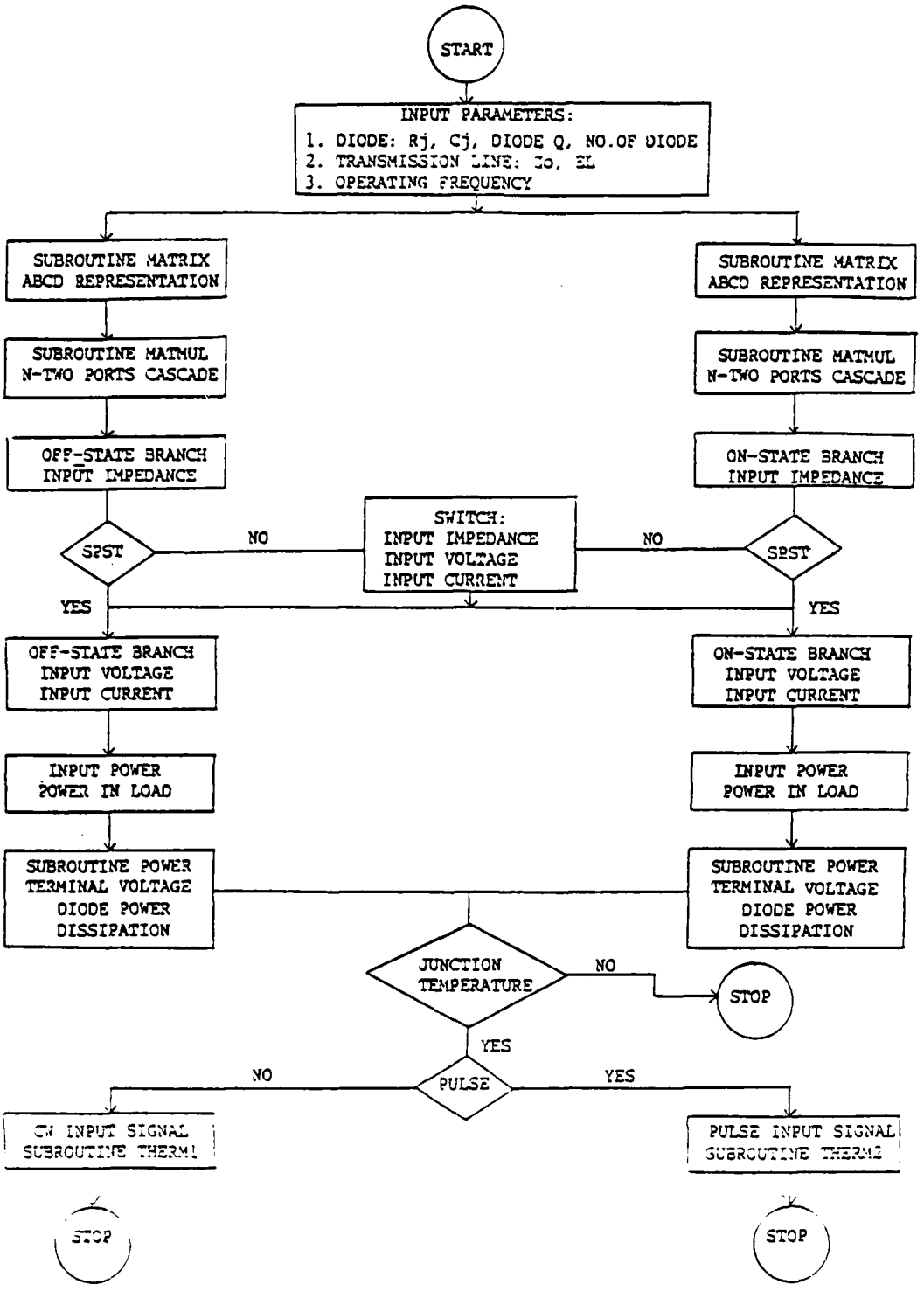


Figure 4.13 Flow Diagram for Calculation of Power Dissipation and Diode Junction Temperature.

$$I_{on} = \frac{I_{in}Z_{inoff}}{Z_{inon}+Z_{inoff}} \qquad \text{(eqn 4.11)}$$

$$I_{off} = \frac{I_{in}Z_{inon}}{Z_{inon}+Z_{inoff}} \qquad \text{(eqn 4.12)}$$

$$= I_{in} - I_{on}$$

where I_{on} is the current flow in switch on-state branch,

I_{off} is the current flow in the switch off-state branch,

Z_{inon} is the input impedance of the switch on-state branch and,

Z_{inoff} is the input impedance of the switch off-state branch.

The final step of nodal voltage and current calculation returns to Figure 4.12(a). In each branch, starting from the leftmost node, currents and voltages in adjacent nodes are calculated by equations 2.24 and 2.25. In this step we obtain the currents flowing in and out of each particular node, as well as the input and output voltages, leading us to the power calculation as in the next section.

2. Power Dissipation in the Individual P-I-N Diode

For the calculation of diode power dissipation in each branch of the switch, we create the subroutine named POWER. In this subroutine, the input currents and input voltage of each branch are the initial input parameters. These currents together with input and output voltages of the diode's node are calculated from equations 2.24 and 2.25. Equation 2.26 is used to calculate the diode power dissipation with its corresponding nodal voltage and current. For the power at load we can use the rightmost nodal current and voltage (I_n, V_n) as inputs to equation 2.27 or using equation 2.28 with the branch input power minus the total of all power dissipation in that branch (include power dissipation in the transmission line sections). The power dissipation in each diode and all the calculated powers are normalized to the power delivered to the load in the switch on-state.

3. Junction Temperature in the Individual P-I-N Diode

The junction temperature of a p-i-n diode is determined by the ambient temperature of the switch and the power dissipation in the diode itself. The ambient temperature is assumed to be constant at about the room temperature. The power dissipation in the diode is a major factor that causes damage to the semiconductor

devices in the switch. From the calculation of power dissipation mentioned in previous section, we can separate the calculation of diode junction temperature into two cases, CW power dissipation and pulsed power dissipation. In the Fortran program, the subroutine THERM1 evaluates the junction temperature of the CW-power case, for the diode mounted on a heat sink. The junction temperature is considered by summing the ambient temperature and the increment of temperature of the diode caused by the input CW-power (equation 3.7). The total thermal resistance, θ_{jc}, of a particular diode is available from the p-i-n diode specification sheet. For the pulsed input-power case, the subroutine THERM2 is used for evaluating the diode junction temperature rise. In this case we assume that the input pulse width is small compared with the thermal time constant, meaning that all the thermal energy is absorbed in the diode, with no energy spreading out to the surroundings. The junction temperature is obtained by summing the ambient temperature and the temperature rise of the junction (equation 3.12), where the temperature rise of the junction is determine by the thermal capacity of the diode active region (HC), the pulse width in microsecond and the power dissipation in the diode (equation 3.11). For the switch design problem, the recommended maximum junction temperature for safe operation is 200°C [Ref. 10: p.290].

4. An Example and Results of Power Dissipation and Diode Junction Temperature Evaluation

Appendix D is the listing of two Fortran programs using for the evaluation of power dissipation and junction temperature in each diode of a single pole single throw switch, and a single pole double throw switch with one or more diodes. These two programs, PSPST and PSPDT, are written for general use. The number of diodes in each branch is an input variable that determines the switch construction (number of transmission line sections). Diode input parameters can be either diode Q or junction resistance and junction capacitance. All input parameters can be entered interactively or in an unformatted input file, and the results of the evaluation are listed in an output file. As an example of power dissipation and junction temperature in a SPDT switch with four MA-4P203 p-i-n diodes, we use PSPDT program in Appendix D2 for the evaluation. From the specification sheet, diode MA-4P203 has 0.15 pF. junction capacitance, 1.5 ohms junction resistance and 30°C/watt total thermal resistance. The value of transmission characteristic impedance and electrical length for each transmission line section are the optimal component values obtained from SPDTD.CKT Touchstone circuit file. For a 100 watt CW power SPDT switch

operating at 10 to 20 GHz frequency range, the results of using PSPDT program are listed in Table 9.

TABLE 9

DIODE POWER DISSIPATION AND JUNCTION TEMPERATURE OF THE 100-WATT CW POWER SWITCH

	ON-STATE				OFF-STATE			
FRE	POWER(watts)		TEMP(°C)		POWER(watts)		TEMP(°C)	
(GHz)	D_1	D_2	D_1	D_2	D_1	D_2	D_1	D_2
10.00	0.814	0.578	39.4	32.3	2.523	0.002	90.7	15.1
12.00	1.124	0.832	48.7	40.0	2.653	0.002	94.6	15.1
14.00	1.486	1.133	59.6	48.9	2.770	0.002	98.1	15.1
16.00	1.908	1.479	72.2	59.4	2.865	0.002	100.9	15.1
18.00	2.407	1.872	87.2	71.2	2.932	0.002	102.9	15.1
20.00	3.003	2.311	104.1	84.3	2.971	0.002	104.1	15.1

From the result in Table 9, we realize that most of the switch power is dissipated in the first diode of each branch, particularly in the switch-off branch. In the switch on-state the power is shared among the two diodes, with the first one dissipating more power. For the whole range of frequencies the first diode of the off-state branch dominates the power dissipation and undergoes the greatest junction temperature rise. The switch can be damaged if the junction temperature exceed its maximum allowable value (200°C). In most diode specification sheets, the maximum power dissipation at the given ambient temperature is given based on the CW-input power to the diode. The CW-input power has more effect in the temperature rise in the diode junction because of the heat accumulated continuously in the junction. For this reason a diode switch with short-duration input power pulses can handle higher peak powers than for CW-input power. For example the MA-4P203 diode has the maximum power handling

capability of 5 watts of CW-input power at 25°C ambient temperature. In Table 9 the designed switch has a maximum power dissipation in the diode of about three watts and 105°C junction temperature (20°C ambient temperature). The result of Table 9 shows that our switch design is capable to handle a 100-watt input CW power. Figure 4.14 shows the plot of normalized powers to one watt output power of an individual diode in both branches.

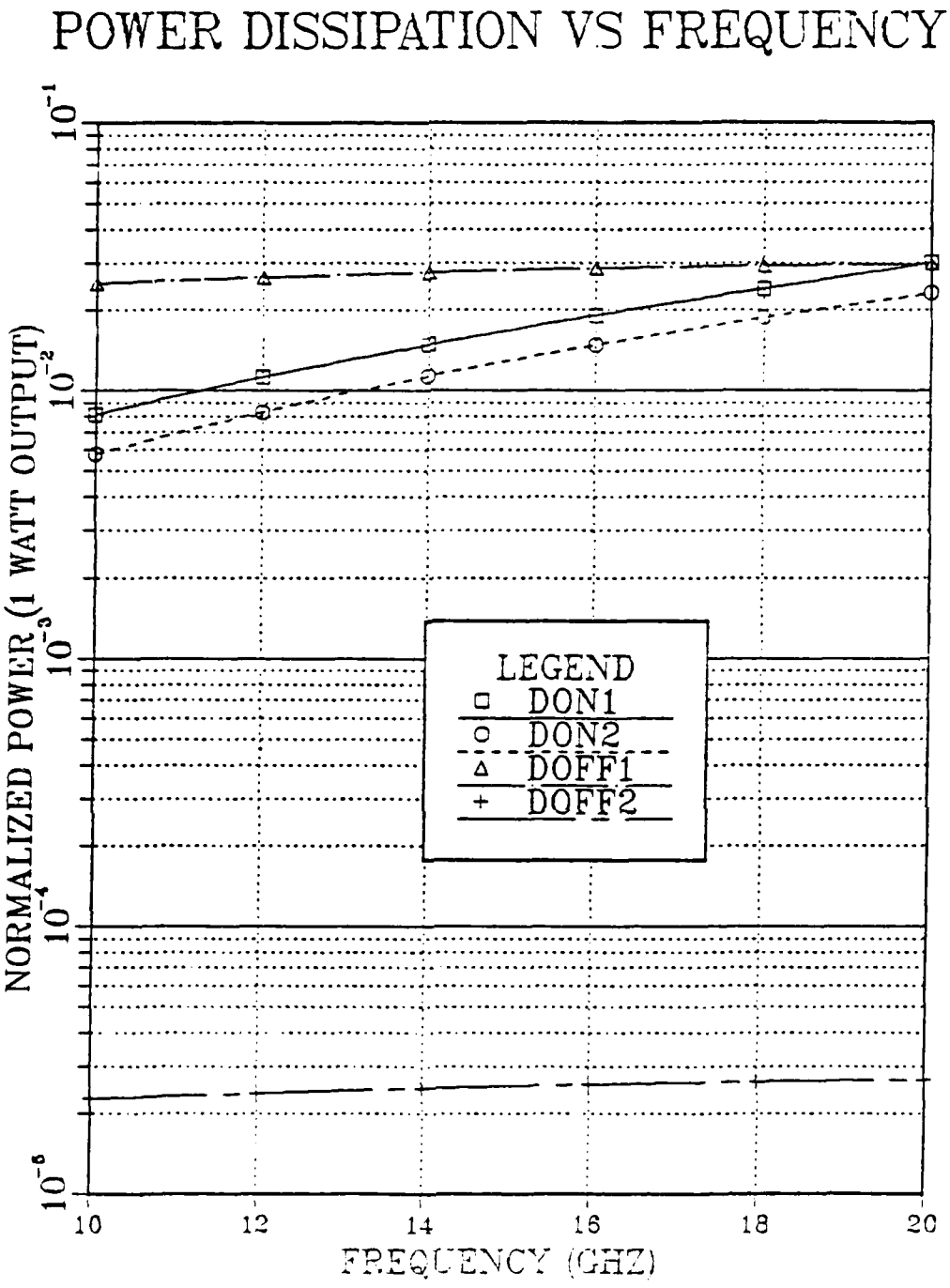


Figure 4.14 Power Dissipation in an Individual Diode.

V. CONCLUSIONS AND REMARKS

In microwave switching design, the CAD program (Touchstone) and Fortran programs, are used for evaluating different types of microwave diode switches in order to obtain their estimated switching characteristics. The selected diode Q as a switching-semiconductor figure of merit can be used as the measure of device switching effectiveness, as shown in chapter 4. For radar applications, a single pole double throw switch with high isolation over a broad operating frequency range is an essential requirement for all radar systems. An addition of more diodes to the switch can improve the switch isolation, while increasing the insertion loss. Figures 5.1 and 5.2 are plots of the switch insertion loss and isolation for switches with one or more diodes. The insertion loss and load isolation in these two figures are produced from the Touchstone circuit file evaluated for the different diode Q values. These two figures are very useful to the designer selecting the number of diodes to be used for specified switch insertion loss and isolation, based on the diode Q value. An appropriate Q value is selected to characterize the behavior of this switch. The Fortran program is used to estimate the power handling capability of the designed switch. The resistor in the diode equivalent circuit plays an important role in its power dissipation. The value of diode Q, from equation 4.1, is a function of both junction capacitance and resistance. One of these two values can be set as an arbitrary parameter, meaning that we can select more than one diode having the same diode Q value. The problem is to select that p-i-n diode which can handle the power dissipation of the switch. One suggestion is to select lower diode resistance to avoid too much power dissipation. However this leads to a trade-off in increased power dissipation in the on-state branch. An example of this is in the previous chapter; the p-i-n diode model number MA-4P203 has the junction resistance of 1.5 ohms and diode Q of 47.15 at 15 GHz, and power dissipation in the on-state branch of the first diode is very close to that of the first diode in the off-state branch (1.68 and 2.32 watts). In some switch applications, it is not desirable to have heat accumulated in the diode junction at all times (both switching state), which may cause shorter diode lifetime. If we select a p-i-n diode which has the same diode Q value but greater junction resistance, for example 2.0 ohms junction resistance, we obtain 3.478 watts power dissipated in the off-state branch and 1.313 watts in the on-state branch. The best way to select the diode for the switch is by using the Fortran

program to estimate the power dissipation in the first diode of each branch, by fixing the diode Q value and varying diode junction resistance and select the satisfactory outcome.

Due to the approximate circuit model used for the diode microwave switch equivalent circuit, the power calculation cannot produce a reliable substitute for measurements in the laboratory. Nonetheless it can reduce the design cost by providing initial guide lines to the designer. On the other hand these assumptions reduce the complexities of the circuit analysis and are mainly employed in the test of different figures of merit. Improvements for more accurate result can be achieved as follows:

1. Using more accurate p-i-n diode equivalent circuit model.
2. Introducing loss in the transmission line sections.

From the knowledge that the first diode in the off-state branch dominates the power dissipation, in a switch circuit design for more efficient switch performance, the diodes used in the circuit can be differed (not necessarily identical). The one closest to the generator should have higher diode Q value (lower junction resistance) in order to dissipate less power, allowing the remaining diodes to share the power dissipation. This method can reduce the maximum power dissipation that occurs in the first diode of the off-state branch, and improve the power handling capability of the switch. We still can use the Touchstone circuit file to evaluate the switch performance by making some necessary modifications to it. The switch optimal insertion loss and isolation are processed by the optimization mode to obtain the optimal switch circuit component values to be used in the power dissipation evaluation with Fortran program.

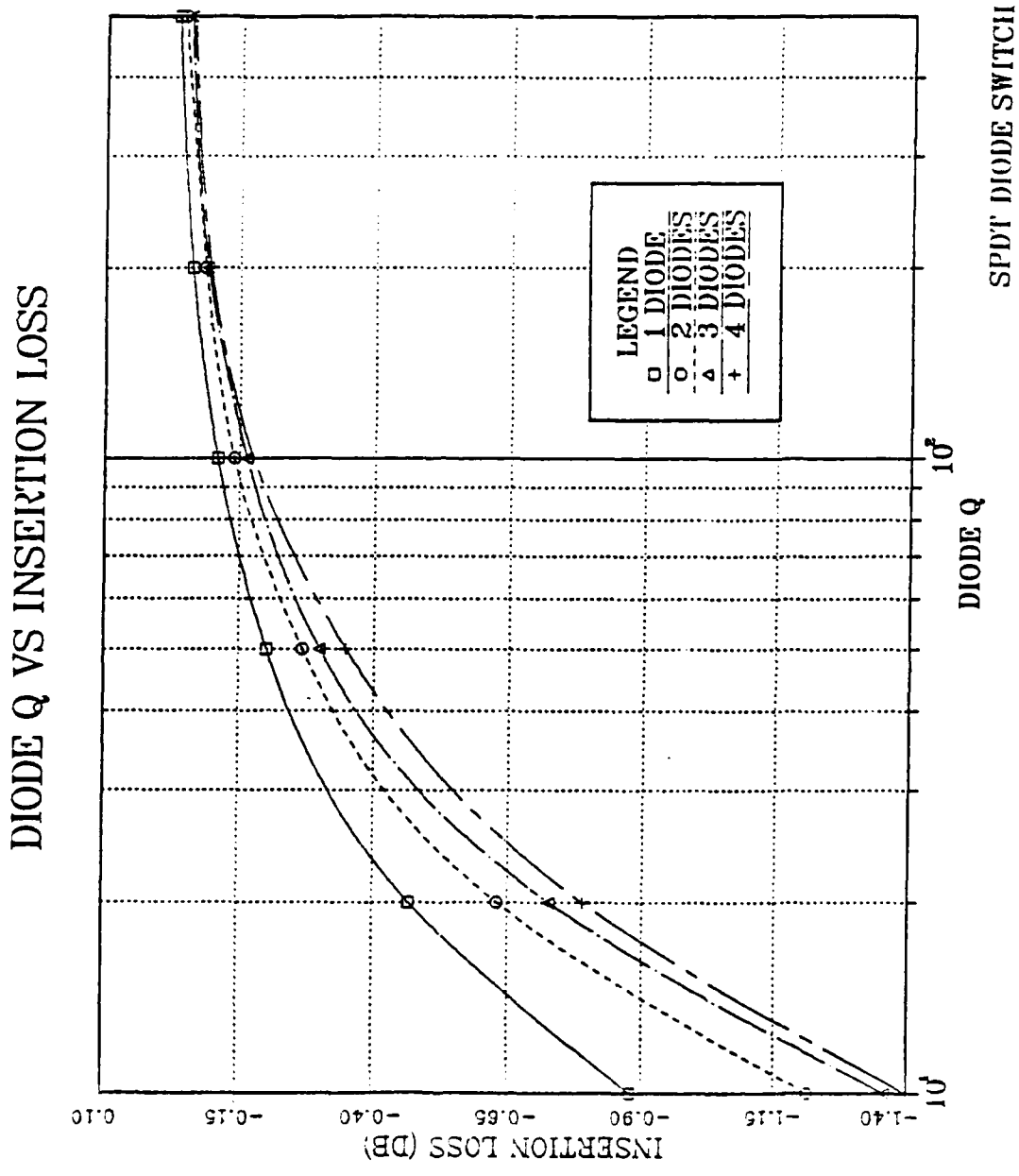


Figure 5.1 Switch Insertion Loss vs Diode Q for Multi-diodes Switch.

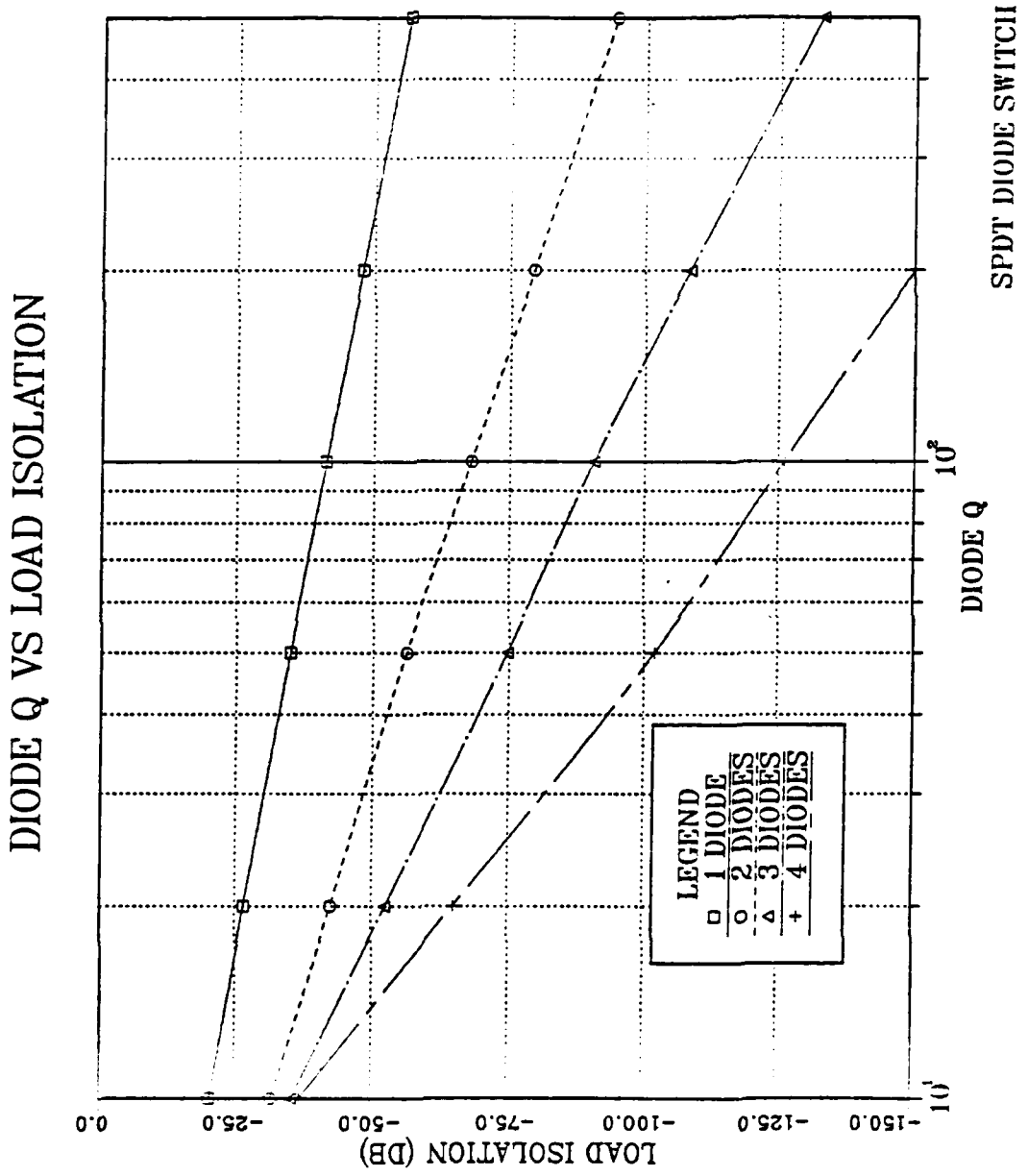


Figure 5.2 Switch Isolation vs Diode Q for Multi-diodes Switch.

APPENDIX A
TOUCHSTONE CIRCUIT FILE FOR SPST SWITCH

This appendix provides the listing of two circuit files using in the Touchstone CAD program for the evaluation switch insertion loss and load isolation for single pole single throw two-diode switches.

A1. SPSTD.CKT evaluate with diode parameters (C_j, R_j).

A2. SPSTQ.CKT evaluate with diode figure of merit (diode Q).

A1. SPSTD.CKT

```
!! SINGLE POLE SINGLE THROW DIODE SWITCH
!! INSERTION LOSS AND LOAD ISOLATION CALCULATION
!! INPUT PARAMETERS :
!! 1. JUNCTION CAPACITANCE, CJ
!! 2. JUNCTION RESISTANCE, RJ
!! 3. CENTER FREQUENCY, F0
!! OUTPUT :
!!  OPTIMIZED TRANSMISSION LINE IMPEDANCE
!!  AND ELECTRICAL LENGTH
!!  MINIMIZED INSERTION LOSS
!!  LOAD ISOLATION
VAR
 ! INPUT PARAMETERS:
 F0 = 15              ! FREQUENCY IN GHz
 CJ = .15             ! JUNCTION CAPACITANCE IN pF
 RJ = 1.5             ! JUNCTION RESISTANCE IN Ohm
 ! OPTIMIZED TRANSMISSION LINE IMPEDANCE(Ohm)
 ZA#30 39.40 90
 ZB#30 38.25 90
 ! OPTIMIZED TRANSMISSION LINE ELECTRICAL LENGTH(Degree)
 EA#30 106.3 120
 EB#30 62.70 120
CKT
 TLIN 1 2 Z^ZA E^EA F^F0
 DEF2P 1 2 SEG1
 TLIN 1 2 Z^ZB E^EB F^F0
 DEF2P 1 2 SEG2
 SRC 1 2 R^RJ C^CJ
 DEF2P 1 2 DON
 RES 1 2 R^RJ
 DEF2P 1 2 DOFF
 ! ON STATE CALCULATION
 SEG1 1 2
 DON 2 0
 SEG2 2 3
 DON 3 0
 SEG1 3 4
 DEF2P 1 4 LINDON
 ! OFF STATE CALCULATION
 SEG1 1 2
 DOFF 2 0
 SEG2 2 3
 DOFF 3 0
 SEG1 3 4
 DEF2P 1 4 LINDOFF
OUT
 LINDON  DB(S21) GR1          ! INSERTION LOSS IN dB
```

```
 LINDOFF DB(S21) GR1A          ! LOAD ISOLATION IN dB
FREQUENCY
 SWEEP 8 22 2                  ! FREQUENCY SWEEP FROM 8 TO 22 GHz
GRID
 GR1  -2  0  .25
 GR1A -20  -80
OPT
 RANGE 10 20
 LINDON DB(S21)=0              ! MINIMIZE INSERTION LOSS
```

A2. SPSTQ.CKT

```
!! SINGLE POLE SINGLE THROW DIODE SWITCH
!! INSERTION LOSS AND LOAD ISOLATION CALCULATION
!! INPUT PARAMETERS :
!! 1. JUNCTION CAPACITANCE, CJ
!! 2. FIGURE OF MERIT (DIODE Q),Q
!! 3. CENTER FREQUENCY, F0
!! OUTPUT :
!!  OPTIMIZED TRANSMISSION LINE IMPEDANCE
!!  AND ELECTRICAL LENGTH
!!  MINIMIZED INSERTION LOSS
!!  LOAD ISOLATION
VAR
 ! INPUT PARAMETERS:
 F0 = 15              ! FREQUENCY IN GHz
 CJ = .15             ! JUNCTION CAPACITANCE IN pF
 Q  = 100             ! FIGURE OF MERIT (DIODE Q)
 ! OPTIMIZED TRANSMISSION LINE IMPEDANCE(Ohm)
 ZA#30 36.66 90
 ZB#30 37.30 90
 ! OPTIMIZED TRANSMISSION LINE ELECTRICAL LENGTH(Degree)
 EA#30 108.3 120
 EB#30 58.7  120
EQN
 RJ = 1000/(2*PI*F0*CJ*Q)      ! JUNCTION RESISTANCE CALCULATION
CKT
 TLIN 1 2 Z^ZA E^EA F^F0
 DEF2P 1 2 SEG1
 TLIN 1 2 Z^ZB E^EB F^F0
 DEF2P 1 2 SEG2
 SRC 1 2 R^RJ C^CJ
 DEF2P 1 2 DON
 RES 1 2 R^RJ
 DEF2P 1 2 DOFF
 ! ON STATE CALCULATION
 SEG1 1 2
 DON 2 0
 SEG2 2 3
 DON 3 0
 SEG1 3 4
 DEF2P 1 4 LINDON
 ! OFF STATE CALCULATION
 SEG1 1 2
 DOFF 2 0
 SEG2 2 3
 DOFF 3 0
 SEG1 3 4
 DEF2P 1 4 LINDOFF
OUT
 LINDON  DB(S21) GR1           ! INSERTION LOSS IN dB
 LINDOFF DB(S21) GR1A          ! LOAD ISOLATION IN dB
FREQUENCY
 SWEEP 8 22 2                  ! FREQUENCY SWEEP FROM 8 TO 22 GHz
GRID
 GR1  -2  0  .25
```

```
 GR1A -20  -80
OPT
 RANGE 10 20
 LINDON DB(S21) = 0            ! MINIMIZE INSERTION LOSS
```

APPENDIX B
TOUCHSTONE CIRCUIT FILE FOR SPDT SWITCH

This appendix provides the listing of two circuit files using in the Touchstone CAD program for the evaluation switch insertion loss and load isolation for single pole double throw four-diode switches.

B1. SPDTD.CKT evaluate with the diode parameters (C_j, R_j).

B2. SPDTQ.CKT evaluate with diode figure of merit (diode Q).

B1. SPDTD.CKT

```
!! SINGLE POLE DOUBLE THROW DIODE SWITCH
!! INSERTION LOSS AND LOAD ISOLATION CALCULATION
!! INPUT PARAMETERS :
!! 1. JUNCTION CAPACITANCE, CJ
!! 2. JUNCTION RESISTANCE, RJ
!! 3. CENTER FREQUENCY, F0
!! 4. TERMINAL LOAD
!! OUTPUT :
!!  OPTIMIZED TRANSMISSION LINE IMPEDANCE
!!  AND ELECTRICAL LENGTH
!!  MINIMIZED INSERTION LOSS
!!  LOAD ISOLATION
VAR
 ! INPUT PARAMETERS:
 F0 = 15              ! FREQUENCY IN GHz
 CJ = .15             ! JUNCTION CAPACITANCE IN pF
 RJ = 1.5             ! JUNCTION RESISTANCE IN Ohm
 RR =  50             ! TERMINAL LOAD IN Ohm
 ! OPTIMIZED TRANSMISSION LINE IMPEDANCE(Ohm)
 ZA#30 46.56 90
 ZB#30 39.06 90
 ! OPTIMIZED TRANSMISSION LINE ELECTRICAL LENGTH(Degree)
 EA#30 93.58 120
 EB#30 32.82 120
CKT
 TLIN 1 2 Z^ZA E^EA F^F0
 DEF2P 1 2 SEG1
 TLIN 1 2 Z^ZB E^EB F^F0
 DEF2P 1 2 SEG2
 SRC 1 2 R^RJ C^CJ
 DEF2P 1 2 DON
 RES 1 2 R^RJ
 DEF2P 1 2 DOFF
 ! ON STATE BRANCH
 SEG1 1 2
 DON 2 0
 SEG2 2 3
 DON 3 0
 SEG1 3 4
 ! OFF STATE BRANCH
 SEG1 1 5
 DOFF 5 0
 SEG2 5 6
 DOFF 6 0
 SEG1 6 7
 ! DEFINE 3 PORTS SWITCH
 DEF3P 1 4 7 SWITCH
```

```
 SWITCH 1 2 3
 RES 3 0 R^RR
 DEF2P 1 2 SWON                ! INSERTION LOSS SWITCH ON STATE
 SWITCH 1 2 3
 RES 2 0 R^RR
 DEF2P 1 3 SWOFF               ! LOAD ISOLATION SWITCH OFF STATE
OUT
 SWON  DB(S21) GR1             ! INSERTION LOSS IN dB
 SWOFF DB(S21) GR1A            ! LOAD ISOLATION IN dB
FREQUENCY
 SWEEP 8 22 2                  ! FREQUENCY SWEEP FROM 8 TO 22 GHz
GRID
 GR1  -2  0  .25
 GR1A -20  -80
OPT
 RANGE 10 20
 LINDON DB(S21)=0              ! MINIMIZE INSERTION LOSS
```

B2. SPDTQ.CKT

```
!! SINGLE POLE DOUBLE THROW DIODE SWITCH
!! INSERTION LOSS AND LOAD ISOLATION CALCULATION
!! INPUT PARAMETERS :
!! 1. JUNCTION CAPACITANCE, CJ
!! 2. FIGURE OF MERIT (DIODE Q),Q
!! 3. CENTER FREQUENCY, F0
!! 4. TERMINAL LOAD, RR
!! OUTPUT :
!!  OPTIMIZED TRANSMISSION LINE IMPEDANCE
!!  AND ELECTRICAL LENGTH
!!  MINIMIZED INSERTION LOSS
!!  LOAD ISOLATION
VAR
 ! INPUT PARAMETERS:
 F0 = 15              ! FREQUENCY IN GHz
 CJ = .20             ! JUNCTION CAPACITANCE IN pF
 Q  = 100             ! FIGURE OF MERIT (DIODE Q)
 RR = 50              ! TERMINAL LOAD IN Ohm
 ! OPTIMIZED TRANSMISSION LINE IMPEDANCE (Ohm)
 ZA#30 36.66 90
 ZB#30 37.30 90
 ! OPTIMIZED TRANSMISSION LINE ELECTRICAL LENGTH (Degree)
 EA#30 108.3 120
 EB#30 58.7  120
EQN
 RJ = 1000/(2*PI*F0*CJ*Q)      ! JUNCTION RESISTANCE CALCULATION
CKT
 TLIN 1 2 Z^ZA E^EA F^F0
 DEF2P 1 2 SEG1
 TLIN 1 2 Z^ZB E^EB F^F0
 DEF2P 1 2 SEG2
 SRC 1 2 R^RJ C^CJ
 DEF2P 1 2 DON
 RES 1 2 R^RJ
 DEF2P 1 2 DOFF
 ! ON STATE BRANCH
 SEG1 1 2
 DON 2 0
 SEG2 2 3
 DON 3 0
 SEG1 3 4
 ! OFF STATE BRANCH
 SEG1 1 5
 DOFF 5 0
 SEG2 5 6
```

```
 DOFF 6 0
 SEG1 6 7
 ! DEFINE 3 PORTS SWITCH
 DEF3P 1 4 7 SWITCH
 SWITCH 1 2 3
 RES 2 0 R^RR
 DEF2P 1 2 SWON                ! INSERTION LOSS SWITCH ON STATE
 SWITCH 1 2 3
 RES 3 0 R^RR
 DEF2P 1 3 SWOFF               ! LOAD ISOLATION SWITCH OFF STATE
OUT
 SWON  DB(S21) GR1             ! INSERTION LOSS IN dB
 SWOFF DB(S21) GR1A            ! LOAD ISOLATION IN dB
FREQUENCY
 SWEEP 8 22 2                  ! FREQUENCY SWEEP FROM 8 TO 22 GHz
GRID
 GR1  -2  0  .25
 GR1A -20  -80
OPT
 RANGE 10 20
 LINDON DB(S21) = 0            ! MINIMIZE INSERTION LOSS
```

APPENDIX C
TOUCHSTONE CIRCUIT FILE FOR NODAL VOLTAGE EVALUATION

This appendix provides the listing of two circuit files using in the Touchstone CAD program for the evaluation of nodal voltages by using voltage-controlled voltage source circuit model for single pole single throw two-diode switches and single pole double throw four-diode switches.

C1. SPSTV.CKT single pole single throw nodal voltage evaluation

C2. SPDTV.CKT single pole double throw nodal voltage evaluation

C1. SPSTD.CKT

```
!! SINGLE POLE SINGLE THROW DIODE SWITCH
!! NODAL VOLTAGE CALCULATION USING VOLTAGE-CONTROLED VOLTAGE SOURCE
!! INPUT PARAMETERS :
!! 1. JUNCTION CAPACITANCE, CJ
!! 2. JUNCTION RESISTANCE, RJ
!! 3. CENTER FREQUENCY, F0
!! 4. TERMINAL LOAD IMPEDANCE, RR
!! 5. TRANSMISSION LINE IMPEDANCE, ZA, ZB
!! 6. TRANSMISSION LINE ELECTRICAL LENGTH, EA, EB
!! OUTPUT:
!!  NORMALIZED NODAL VOLTAGE OF THE INTERESTED NODE
VAR
 ! INPUT PARAMETERS:
 F0 = 15              ! FREQUENCY IN GHz
 CJ = .15             ! JUNCTION CAPACITANCE IN pF
 RJ = 1.5             ! JUNCTION RESISTANCE  IN Ohm
 RR = 50              ! TERMINAL LOAD IMPEDANCE IN Ohm
 ! TRANSMISSION LINE IMPEDANCE(Ohm)
 ZA  = 36.66
 ZB  = 37.30
 ! TRANSMISSION LINE ELECTRICAL LENGTH(Degree)
 EA  = 108.3
 EB  = 58.7
CKT
 TLIN 1 2 Z^ZA E^EA F^F0
 DEF2P 1 2 SEG1
 TLIN 1 2 Z^ZB E^EB F^F0
 DEF2P 1 2 SEG2
 CAP 1 2 C^CJ
 DEF2P DCJ
 RES 1 2 R^RJ
 DEF2P 1 2 DRJ
 ! ON STATE CALCULATION
 SEG1 1 2
 DCJ 2 5
 DRJ 5 0
 SEG2 2 3
 DCJ 3 6
 DRJ 6 0
 SEG 3 4
 RES 4 0 R^RR
 VCVS 4 7 0 0 M=-.5 A=0 R1=1E8 R2=0 F=0 T=0
 VCVS 5 8 0 0 M=-.5 A=0 R1=1E8 R2=0 F=0 T=0
 VCVS 6 9 0 0 M=-.5 A=0 R1=1E8 R2=0 F=0 T=0
 DEF4P 1 7 8 9  OUTV1
```

```
 ! OFF STATE CALCULATION
 SEG1 11 12
 DRJ 12 0
 SEG2 12 13
 DRJ 13 0
 SEG1 13 14
 RES 14 0 R^RR
 VCVS 14 17 0 0 M=-.5 A=0 R1=1E8 R2=0 F=0 T=0
 VCVS 12 18 0 0 M=-.5 A=0 R1=1E8 R2=0 F=0 T=0
 VCVS 13 19 0 0 M=-.5 A=0 R1=1E8 R2=0 F=0 T=0
 DEF4P 11 17 18 19 OUTV2
OUT
 ! NORMALIZED NODAL VOLTAGE
 OUTV1 MAG(S21) GR1
 OUTV1 MAG(S31) GR1A
 OUTV1 MAG(S41) GR1A
 OUTV2 MAG(S21) GR2
 OUTV2 MAG(S31) GR1A
 OUTV2 MAG(S41) GR2
FREQUENCY
 SWEEP 8 22 2                    ! FREQUENCY SWEEP FROM 8 TO 22 GHz
GRID
 RANGE 8  22  2
 GR1   0  .5  1
 GR1A  0  .15  .3
 GR2   0  .001  .0001
```

C2. SPDTV.CKT

```
!! SINGLE POLE DOUBLE THROW DIODE SWITCH
!! NODAL VOLTAGE CALCULATION USING VOLTAGE-CONTROLED VOLTAGE SOURCE
!! INPUT PARAMETERS :
!! 1. JUNCTION CAPACITANCE, CJ
!! 2. JUNCTION RESISTANCE, RJ
!! 3. CENTER FREQUENCY, F0
!! 4. TERMINAL LOAD IMPEDANCE, RR
!! 5. TRANSMISSION LINE IMPEDANCE, ZA, ZB
!! 6. TRANSMISSION LINE ELECTRICAL LENGTH, EA, EB
!! OUTPUT :
!!  NORMALIZED NODAL VOLTAGE OF THE INTERESTED NODE
VAR
 ! INPUT PARAMETERS:
 F0 = 15              ! FREQUENCY IN GHz
 CJ = .20             ! JUNCTION CAPACITANCE IN pF
 RJ = 1.5             ! JUNCTION RESISTANCE IN Ohm
 RR = 50              ! TERMINAL LOAD IMPEDANCE IN Ohm
 ! TRANSMISSION LINE IMPEDANCE(Ohm)
 ZA  = 35.90
 ZB  = 47.36
 ! TRANSMISSION LINE ELECTRICAL LENGTH(Degree)
 EA  = 101.20
 EB  = 34.7
CKT
 TLIN 1 2 Z^ZA E^EA F^F0
 DEF2P 1 2 SEG1
 TLIN 1 2 Z^ZB E^EB F^F0
 DEF2P 1 2 SEG2
 CAP 1 2 C^CJ
 DEF2P DCJ
 RES 1 2 R^RJ
 DEF2P 1 2 DRJ
 ! ON STATE CALCULATION
 SEG1 1 2
```

```
 DCJ 2 8
 DRJ 8 0
 SEG2 2 3
 DCJ 3 9
 DRJ 9 0
 SEG 3 4
 RES 4 0 R^RR
 ! OFF STATE CALCULATION
 SEG1 1 5
 DRJ 5 0
 SEG2 5 6
 DRJ 6 0
 SEG1 6 7
 RES 7 0 R^RR
 VCVS 4 10 0 0 M=-.5 A=0 R1=1E8 R2=0 F=0 T=0
 VCVS 8 11 0 0 M=-.5 A=0 R1=1E8 R2=0 F=0 T=0
 VCVS 5 12 0 0 M=-.5 A=0 R1=1E8 R2=0 F=0 T=0
 DEF4P 1 10 11 12 OUTV1
OUT
 ! NORMALIZED NODAL VOLTAGE
 OUTV1 MAG(S21) GR1
 OUTV1 MAG(S31) GR1A
 OUTV1 MAG(S41) GR1A
FREQUENCY
 SWEEP 8 22 2                    ! FREQUENCY SWEEP FROM 8 TO 22 GHz
GRID
 RANGE 8  22  2
 GR1   0  .5  1
 GR1A  0  .5  .1
```

APPENDIX D

FORTRAN PROGRAM FOR DIODE POWER AND HEATING CALCULATIONS

This appendix provides the listing of two Fortran programs written for the evaluation of power dissipation and junction temperature in the individual diode of the single pole single throw and single pole double diode switches.

D1. PSPST diode power dissipation and junction temperature of a single pole single throw diode switch.

D2. PSPDT diode power dissipation and junction temperature of a single pole double throw diode switch.

D1. PSPST

```
      CHARACTER*1 ANSWER
      CHARACTER*13 FILE
      CHARACTER*3 SELECT
      CHARACTER*1 TYPE
      INTEGER I,NPORT
      REAL TA,TR,HC,TJON(10),TJOFF(10),DT
      REAL*8 FRE,Q,CJ,EL(10),RR,PI,PIN,PON,POFF,PLON,PLOFF
      REAL*8 PDON(10),PDOFF(10),AMP,VDONM,PEX
      COMPLEX*16 VIN,ZOUT,Z(10),ZINON,ZINOFF,ZIN,IIN,ION,IOFF,ILON,VLON
      COMPLEX*16 ILOFF,VLOFF,VON,VOFF,VS,ZS
      COMPLEX*16 GPI(2,2,20),GP(2,2,20),GNI(2,2,20),GN(2,2,20)
      COMPLEX*16 IDON(10),IDOFF(10),VDON(10)
      COMPLEX*16 VDOFF(10)
      OPEN(UNIT=2,FILE='OUTPUT')
      PI = 3.1415926536
5     WRITE(6,*)'POWER DISSIPATION AND JUNCTION TEMPERATURE EVALUATION'
      WRITE(6,*)'OF SPST DIODE SWITCH '
      WRITE(6,*)'"PRESS ANY KEY AND RETURN" TO CONTINUE,"Q AND RETURN"TO
     * QUIT'
      READ(5,10)ANSWER
10    FORMAT(A1)
      IF(ANSWER.EQ.'Q')STOP
      WRITE(6,*)'ENTER"0"TO READ INPUT FROM FILE,"1"TO ENTER INPUTS INTE
     *RACTIVELY'
      READ(5,*)NUM
      IF(NUM.NE.0.AND.NUM.NE.1) GOTO 5
      IF(NUM.EQ.0)THEN
      MN = 1
      ELSE
      MN = 5
      ENDIF
      IF(NUM.EQ.0)THEN
      WRITE(6,*)'ENTER THE NAME OF INPUT FILE'
      READ(5,15)FILE
      OPEN(UNIT=1,FILE=FILE)
15    FORMAT(A13)
      ENDIF
      IF(NUM.EQ.1)THEN
20    WRITE(6,*)'WHAT TYPE OF INPUT SIGNAL "PULSE" OR "CW" ? '
      WRITE(6,*)'FOR "PULSE" INPUT ENTER "P" '
      WRITE(6,*)'FOR "CW" INPUT ENTER "C" '
      WRITE(6,*)'DO NOT EVALUATE JUNCTION TEMPERATURE ENTER "N" '
```

```
      ENDIF
      READ(MN,11)TYPE
25    FORMAT(A1)
      IF(TYPE.NE.'P'.AND.TYPE.NE.'C'.AND.TYPE.NE.'N')GOTO 20
      IF(TYPE.EQ.'N')GOTO 30
      IF(TYPE.EQ.'C')THEN
      IF(NUM.EQ.1)WRITE(6,*)'ENTER AMBIENT TEMPERATURE (DEGREE C)'
      READ(MN,*)TA
      IF(NUM.EQ.1)WRITE(6,*)'TOTAL THERMAL RESISTANCE (DEGREE C/WATT)'
      READ(MN,*)TR
      ELSE
      IF(NUM.EQ.1)WRITE(6,*)'ENTER AMBIENT TEMPERATURE (DEGREE C)'
      READ(MN,*)TA
      IF(NUM.EQ.1)WRITE(6,*)'ENTER THERMAL CAPACITY OF OF I-REGION (MICR
     *O-JOULE/DEGREE C)'
      READ(MN,*)HC
      IF(NUM.EQ.1)WRITE(6,*)'ENTER THE PULSE DURATION (MICRO-SECOND)'
      READ(MN,*)DT
      ENDIF
30    IF(NUM.EQ.1)THEN
      WRITE(6,*)'IS THIS EVALUATION USE THE FIGURE OF MERIT,DIODE Q'
      WRITE(6,*)'ANSWER "YES" OR "NO"'
      ENDIF
      READ(MN,35)SELECT
35    FORMAT(A3)
      IF(SELECT.NE.'YES'.AND.SELECT.NE.'NO')GOTO 30
      IF(SELECT.EQ.'YES')THEN
      IF(NUM.EQ.1)WRITE(6,*)'ENTER THE VALUE OF DIODE Q '
      READ(MN,*)Q
      IF(NUM.EQ.1)WRITE(6,*)'ENTER THE VALUE OF JUNCTION CAPACITANCE (PF)
     *'
      READ(MN,*)CJ
      IF(NUM.EQ.1)WRITE(6,*)'ENTER THE EVALUATE FREQUENCY (GHZ)'
      READ(MN,*)FRE
      RR = 1000/(2*PI*FRE*Q*CJ)
      ELSE
      IF(NUM.EQ.1)WRITE(6,*)'ENTER THE VALUE OF JUNCTION CAPACITANCE (PF)
     *'
      READ(MN,*)CJ
      IF(NUM.EQ.1)WRITE(6,*)'ENTER THE EVALUATE FREQUENCY (GHZ)'
      READ(MN,*)FRE
      IF(NUM.EQ.1)WRITE(6,*)'ENTER THE VALUE OF JUNCTION RESISTANCE (OHM
     *)'
      READ(MN,*)RR
      Q = 1000/(2*PI*FRE*RR*CJ)
      ENDIF
      VS = (1,0)
      ZS = (50,0)
      IF(NUM.EQ.1)WRITE(6,*)'ENTER NUMBER OF DIODES IN EACH BRANCH'
      READ(MN,*)ND
      IF(NUM.EQ.1)WRITE(6,*)'ENTER THE EXPECT POWER AT LOAD (WATT)'
      READ(MN,*)PEX
      IF(NUM.EQ.1)WRITE(6,*)'ENTER THE OUTPUT IMPEDANCE (COMPLEX)'
      READ(MN,*)ZOUT
      NSEG = ND+1
      DO 40 I =1,NSEG
      IF(NUM.EQ.1)WRITE(6,*)'TRANSMISSION SEGMENT NUMBER',I
      IF(NUM.EQ.1)WRITE(6,*)'ENTER IMPEDANCE OF TRANSMISSION LINE (COMPL
     *EX)'
      READ(MN,*)Z(I)
      IF(NUM.EQ.1)WRITE(6,*)'ENTER ELECTRICAL LENGTH (DEGREE)'
      READ(MN,*)EL(I)
      EL(I) = EL(I)*PI/180
40    CONTINUE
      NPORT = ND+NSEG


C     ON STATE CALCULATION
      CALL MATRIX(RR,CJ,Z,EL,NSEG,ND,FRE,GP(1,1,1))
      DO 45 K =1,NPORT
```

```
      IF(K.EQ.1)THEN
      GPI(1,1,1) = GP(1,1,1)
      GPI(1,2,1) = GP(1,2,1)
      GPI(2,1,1) = GP(2,1,1)
      GPI(2,2,1) = GP(2,2,1)
      ELSE
      CALL MATMUL(GPI(1,1,K-1),GP(1,1,K),2,2,2,GPI(1,1,K))
      ENDIF
45    CONTINUE
      ZINON = (GPI(1,1,NPORT)*ZOUT+GPI(1,2,NPORT))/(GPI(2,1,NPORT)*ZOUT
     #+GPI(2,2,NPORT))

C     OFF STATE CALCULATION
      CALL MATRIX(RR,0.D0,Z,EL,NSEG,ND,FRE,GN(1,1,1))
      DO 50 N =1, NPORT
      IF(N.EQ.1)THEN
      GNI(1,1,1) = GN(1,1,1)
      GNI(1,2,1) = GN(1,2,1)
      GNI(2,1,1) = GN(2,1,1)
      GNI(2,2,1) = GN(2,2,1)
      ELSE
      CALL MATMUL(GNI(1,1,N-1),GN(1,1,N),2,2,2,GNI(1,1,N))
      ENDIF
50    CONTINUE
      ZINOFF =(GNI(1,1,NPORT)*ZOUT+GNI(1,2,NPORT))/(GNI(2,1,NPORT)*ZOUT
     #+GNI(2,2,NPORT))

C     ON-OFF STATE
      VON  =  ZINON*VS/(ZINON+VS)
      ION  =  VON/ZINON
      VOFF =  ZINOFF*VS/(ZINOFF+VS)
      IOFF =  VOFF/ZINOFF
      PON  = 0.5*REAL(VON*DCONJG(ION))
      POFF = 0.5*REAL(VOFF*DCONJG(IOFF))
      ILON = GPI(1,1,NPORT)*ION-GPI(2,1,NPORT)*VON
      VLON = GPI(2,2,NPORT)*VON-GPI(1,2,NPORT)*ION
      PLON = PON-0.5*REAL(VON*DCONJG(ION)-VLON*DCONJG(ILON))
      AMP  = PEX/PLON
      WRITE(2,55) FRE
      WRITE(2,60) Q
      WRITE(2,65) ND
      WRITE(2,70) CJ
      WRITE(2,75) RR
      WRITE(2,85) PON*AMP
      WRITE(2,90) POFF*AMP
      WRITE(2,95) PLON*AMP
      ILOFF = GNI(1,1,NPORT)*IOFF-GNI(2,1,NPORT)*VOFF
      VLOFF = GNI(2,2,NPORT)*VOFF-GNI(1,2,NPORT)*IOFF
      PLOFF = POFF-0.5*REAL(VOFF*DCONJG(IOFF)-VLOFF*DCONJG(ILOFF))
      WRITE(2,100) PLOFF*AMP
55    FORMAT(' ','OPERATING FREQUENCY',3X,F5.2,2X,'GHZ')
60    FORMAT(' ','FIGURE OF MERIT (DIODE Q)',3X,F8.3)
65    FORMAT(' ','TOTAL NUMBER OF DIODE IN EACH BRANCH',2X,I2)
70    FORMAT(' ','DIODE JUNCTION CAPACITANCE',3X,F5.3,2X,'PF')
75    FORMAT(' ','DIODE JUNCTION RESISTANCE',3X,F5.3,2X,'OHM')
85    FORMAT(' ','POWER IN ON STATE ',2X,F10.2,3X,'WATTS')
90    FORMAT(' ','POWER IN OFF STATE',1X,F10.2,3X,'WATTS')
95    FORMAT(' ','POWER DELIVER TO THE LOAD IN ON STATE',F10.2,3X,'WATTS
     *')
100   FORMAT(' ','POWER DELIVER TO THE LOAD IN OFF STATE',F10.6,3X,'WATT
     *S')

C     POWER DISSIPATED IN ON STATE BRANCH
      CALL POWER(GP(1,1,1),ION,VON,NPORT,PDON,IDON,VDON)
      WRITE(2,*)'POWER DISSIPATION IN DIODE ON STATE'
      DO 105 I = 2,2*ND,2
      WRITE(2,115)I/2,PDON(I)*AMP
```

```
105     CONTINUE

C       POWER DISSIPATED IN OFF STATE BRANCH
        CALL POWER(GN(1,1,1),IOFF,VOFF,NPORT,PDOFF,IDOFF,VDOFF)
        WRITE(2,*)'POWER DISSIPATION IN DIODE OFF STATE'
        DO 110 J = 2,2*ND,2
        WRITE(2,115)J/2,PDOFF(J)*AMP
110     CONTINUE
115     FORMAT(' ','POWER DISSIPATED IN DIODE NO.',1X,I2,2X,F10.5,2X,'WATT
       *S')

C       JUNCTION TEMPERATURE CALCULATION
C       JUNCTION TEMPERATURE IN ON STATE BRANCH
        IF(TYPE.EQ.'N')STOP
        IF(TYPE.EQ.'C')THEN
        CALL THERM1(ND,TJON,PDON,AMP,TA,TR)
        ELSE
        CALL THERM2(ND,TJON,PDON,AMP,TA,DT,HC)
        ENDIF
        WRITE(2,*)'JUNCTION TEMPERATURE ON STATE BRANCH'
        DO 120 I = 1,ND
        WRITE(2,82)I,TJON(I)
120     CONTINUE
C       JUNCTION TEMPERATURE IN OFF STATE BRANCH
        WRITE(2,*)'JUNCTION TEMPERATURE OFF STATE BRANCH'
        IF(TYPE.EQ.'C')THEN
        CALL THERM1(ND,TJOFF,PDOFF,AMP,TA,TR)
        ELSE
        CALL THERM2(ND,TJOFF,PDOFF,AMP,TA,DT,HC)
        ENDIF
        DO 125 J = 1,ND
        WRITE(2,130)J,TJOFF(J)
125     CONTINUE
130     FORMAT(' ','JUNCTION TEMPERATURE DIODE NO.',2X,I2,2X,F6.2,2X,'DEGR
       *EE C')
        STOP
        END


c                               SUBROUTINE MATRIX
        SUBROUTINE MATRIX(RR,CJ,Z,EL,NSEG,ND,FRE,GP)
        REAL*8 RR,CJ,EL(10),FRE,PI
        COMPLEX*16 Z(10),Z1
        COMPLEX*16 G(2,2,20),G1(2,2,20),GP(2,2,20)
        PI = 3.1415926536
        DO 10 K = 1,NSEG
        G(1,1,K) = DCMPLX(COS(EL(K)),0.D0)
        G(1,2,K) = DCMPLX(0.D0,1.D0)*Z(K)*DCMPLX(SIN(EL(K)),0.D0)
        G(2,1,K) = DCMPLX(0.D0,1.D0)/Z(K)*DCMPLX(SIN(EL(K)),0.D0)
        G(2,2,K) = G(1,1,K)
10      CONTINUE
        DO 20 L=1,ND
        IF(CJ.EQ.0.D0)THEN
        Z1 = DCMPLX(RR,0.D0)
        ELSE
        Z1 = DCMPLX(RR,-1000/(2*PI*FRE*CJ))
        ENDIF
        G1(1,1,L) = DCMPLX(1.D0,0.D0)
        G1(1,2,L) = DCMPLX(0.D0,0.D0)
        G1(2,1,L) = 1/Z1
        G1(2,2,L) = G1(1,1,L)
20      CONTINUE
        DO 30 M =1,NSEG
        N = 2*M-1
        GP(1,1,N) = G(1,1,M)
        GP(1,2,N) = G(1,2,M)
        GP(2,1,N) = G(2,1,M)
        GP(2,2,N) = G(2,2,M)
30      CONTINUE
        DO 40 I =1,ND
```

```
      J = 2*I
      GP(1,1,J) = G1(1,1,I)
      GP(1,2,J) = G1(1,2,I)
      GP(2,1,J) = G1(2,1,I)
      GP(2,2,J) = G1(2,2,I)
40    CONTINUE
      RETURN
      END

C                          SUBROUTINE MATMUL
      SUBROUTINE MATMUL(AA,BB,NN,MM,RR,CC)
      INTEGER NN,MM,RR
      COMPLEX*16 AA(2,2,1),BB(2,2,1),CC(2,2,1)
      DO 10 I = 1,NN
      DO 20 J = 1,RR
      CC(I,J,1) = 0
      DO 30 K =1,MM
      CC(I,J,1) = CC(I,J,1) + AA(I,K,1)*BB(K,J,1)
30    CONTINUE
20    CONTINUE
10    CONTINUE
      RETURN
      END


C                          SUBROUTINE POWER
      SUBROUTINE POWER(G,I,V,N,PD,IID,VID)
      REAL*8 PD(10)
      COMPLEX*16 G(2,2,20),V,I,IID(20),VID(20),IOD(20),VOD(20)
      DO 10 J=2,N,2
      IID(J) = G(1,1,J-1)*I - G(2,1,J-1)*V
      VID(J) = G(2,2,J-1)*V - G(1,2,J-1)*I
      IOD(J) = G(1,1,J)*IID(J) - G(2,1,J)*VID(J)
      VOD(J) = G(2,2,J)*VID(J) - G(1,2,J)*IID(J)
      PD(J)  = 0.5*REAL(VID(J)*DCONJG(IID(J))-VOD(J)*DCONJG(IOD(J)))
      I = IOD(J)
      V = VOD(J)
10    CONTINUE
      RETURN
      END


C                          SUBROUTINE THERM1
      SUBROUTINE THERM1(ND,TJ,PD,AMP,TA,TR)
      INTEGER ND
      REAL TJ(10),AMP,TA,TR
      REAL*8 PD(10)
      DO 5 I=1,ND
      TJ(I) = TA + (PD(I*2)*AMP)*TR
5     CONTINUE
      RETURN
      END


C                          SUBROUTINE THERM2
      SUBROUTINE THERM2(ND,TJ,PD,AMP,TA,DT,HC)
      INTEGER ND
      REAL TJ(10),AMP,TA,DT,HC
      REAL*8 PD(10)
      DO 5 J =1,ND
      TJ(J) = TA + (PD(J*2)*AMP)*DT/HC
5     CONTINUE
      RETURN
      END
```

D2.PSPDT

```
      CHARACTER*1 ANSWER
      CHARACTER*13 FILE
      CHARACTER*3 SELECT
      CHARACTER*1 TYPE
      INTEGER I,NPORT
      REAL TA,TR,HC,TJON(10),TJOFF(10),DT
      REAL*8 FRE,Q,CJ,EL(10),RR,PI,PIN,PON,POFF,PLON,PLOFF
      REAL*8 PDON(10),PDOFF(10),AMP,VDONM,PEX
      COMPLEX*16 VIN,ZOUT,Z(10),ZINON,ZINOFF,ZIN,IIN,ION,IOFF,ILON,VLON
      COMPLEX*16 ILOFF,VLOFF,VON,VOFF,VS,ZS
      COMPLEX*16 GPI(2,2,20),GP(2,2,20),GNI(2,2,20),GN(2,2,20)
      COMPLEX*16 IDON(10),IDOFF(10),VDON(10)
      COMPLEX*16 VDOFF(10)
      OPEN(UNIT=2,FILE='OUTPUT')
      PI = 3.1415926536
5     WRITE(6,*)'POWER DISSIPATION AND JUNCTION TEMPERATURE EVALUATION'
      WRITE(6,*)'OF SPDT DIODE SWITCH '
      WRITE(6,*)'"PRESS ANY KEY AND RETURN" TO CONTINUE,"Q AND RETURN"TO
     * QUIT'
      READ(5,10)ANSWER
10    FORMAT(A1)
      IF(ANSWER.EQ.'Q')STOP
      WRITE(6,*)'ENTER"0"TO READ INPUT FROM FILE,"1"TO ENTER INPUTS INTE
     *RACTIVELY'
      READ(5,*)NUM
      IF(NUM.NE.0.AND.NUM.NE.1) GOTO 5
      IF(NUM.EQ.0)THEN
      MN = 1
      ELSE
      MN = 5
      ENDIF
      IF(NUM.EQ.0)THEN
      WRITE(6,*)'ENTER THE NAME OF INPUT FILE'
      READ(5,15)FILE
      OPEN(UNIT=1,FILE=FILE)
15    FORMAT(A13)
      ENDIF
      IF(NUM.EQ.1)THEN
20    WRITE(6,*)'WHAT TYPE OF INPUT SIGNAL "PULSE" OR "CW" ? '
      WRITE(6,*)'FOR "PULSE" INPUT ENTER "P" '
      WRITE(6,*)'FOR "CW" INPUT ENTER "C" '
      WRITE(6,*)'DO NOT EVALUATE JUNCTION TEMPERATURE ENTER "N" '
      ENDIF
      READ(MN,11)TYPE
25    FORMAT(A1)
      IF(TYPE.NE.'P'.AND.TYPE.NE.'C'.AND.TYPE.NE.'N')GOTO 20
      IF(TYPE.EQ.'N')GOTO 30
      IF(TYPE.EQ.'C')THEN
      IF(NUM.EQ.1)WRITE(6,*)'ENTER AMBIENT TEMPERATURE (DEGREE C)'
      READ(MN,*)TA
      IF(NUM.EQ.1)WRITE(6,*)'TOTAL THERMAL RESISTANCE (DEGREE C/WATT)'
      READ(MN,*)TR
      ELSE
      IF(NUM.EQ.1)WRITE(6,*)'ENTER AMBIENT TEMPERATURE (DEGREE C)'
      READ(MN,*)TA
      IF(NUM.EQ.1)WRITE(6,*)'ENTER THERMAL CAPACITY OF OF I-REGION (MICR
     *O-JOULE/DEGREE C)'
      READ(MN,*)HC
      IF(NUM.EQ.1)WRITE(6,*)'ENTER THE PULSE DURATION (MICRO-SECOND)'
      READ(MN,*)DT
      ENDIF
```

```
30      IF(NUM.EQ.1)THEN
        WRITE(6,*)'IS THIS EVALUATION USE THE FIGURE OF MERIT,DIODE Q'
        WRITE(6,*)'ANSWER "YES" OR "NO"'
        ENDIF
        READ(MN,35)SELECT
35      FORMAT(A3)
        IF(SELECT.NE.'YES'.AND.SELECT.NE.'NO')GOTO 30
        IF(SELECT.EQ.'YES')THEN
        IF(NUM.EQ.1)WRITE(6,*)'ENTER THE VALUE OF DIODE Q '
        READ(MN,*)Q
        IF(NUM.EQ.1)WRITE(6,*)'ENTER THE VALUE OF JUNCTION CAPACITANCE (PF)
       *'
        READ(MN,*)CJ
        IF(NUM.EQ.1)WRITE(6,*)'ENTER THE EVALUATE FREQUENCY (GHZ)'
        READ(MN,*)FRE
        RR = 1000/(2*PI*FRE*Q*CJ)
        ELSE
        IF(NUM.EQ.1)WRITE(6,*)'ENTER THE VALUE OF JUNCTION CAPACITANCE (PF)
       *'
        READ(MN,*)CJ
        IF(NUM.EQ.1)WRITE(6,*)'ENTER THE EVALUATE FREQUENCY (GHZ)'
        READ(MN,*)FRE
        IF(NUM.EQ.1)WRITE(6,*)'ENTER THE VALUE OF JUNCTION RESISTANCE (OHM
       *)'
        READ(MN,*)RR
        Q = 1000/(2*PI*FRE*RR*CJ)
        ENDIF
        VS = (1,0)
        ZS = (50,0)
        IF(NUM.EQ.1)WRITE(6,*)'ENTER NUMBER OF DIODES IN EACH BRANCH'
        READ(MN,*)ND
        IF(NUM.EQ.1)WRITE(6,*)'ENTER THE EXPECT POWER AT LOAD (WATT)'
        READ(MN,*)PEX
        IF(NUM.EQ.1)WRITE(6,*)'ENTER THE OUTPUT IMPEDANCE (COMPLEX)'
        READ(MN,*)ZOUT
        NSEG = ND+1
        DO 40 I =1,NSEG
        IF(NUM.EQ.1)WRITE(6,*)'TRANSMISSION SEGMENT NUMBER',I
        IF(NUM.EQ.1)WRITE(6,*)'ENTER IMPEDANCE OF TRANSMISSION LINE (COMPL
       *EX)'
        READ(MN,*)Z(I)
        IF(NUM.EQ.1)WRITE(6,*)'ENTER ELECTRICAL LENGTH (DEGREE)'
        READ(MN,*)EL(I)
        EL(I) = EL(I)*PI/180
40      CONTINUE
        NPORT = ND+NSEG

C       ON STATE CALCULATION
        CALL MATRIX(RR,CJ,Z,EL,NSEG,ND,FRE,GP(1,1,1))
        DO 45 K =1,NPORT
        IF(K.EQ.1)THEN
        GPI(1,1,1) = GP(1,1,1)
        GPI(1,2,1) = GP(1,2,1)
        GPI(2,1,1) = GP(2,1,1)
        GPI(2,2,1) = GP(2,2,1)
        ELSE
        CALL MATMUL(GPI(1,1,K-1),GP(1,1,K),2,2,2,GPI(1,1,K))
        ENDIF
45      CONTINUE
        ZINON = (GPI(1,1,NPORT)*ZOUT+GPI(1,2,NPORT))/(GPI(2,1,NPORT)*ZOUT
       #+GPI(2,2,NPORT))

C       OFF STATE CALCULATION
        CALL MATRIX(RR,0.D0,Z,EL,NSEG,ND,FRE,GN(1,1,1))
        DO 50 N =1, NPORT
        IF(N.EQ.1)THEN
        GNI(1,1,1) = GN(1,1,1)
        GNI(1,2,1) = GN(1,2,1)
```

```
      GNI(2,1,1) = GN(2,1,1)
      GNI(2,2,1) = GN(2,2,1)
      ELSE
      CALL MATMUL(GNI(1,1,N-1),GN(1,1,N),2,2,2,GNI(1,1,N))
      ENDIF
50    CONTINUE
      ZINOFF =(GNI(1,1,NPORT)*ZOUT+GNI(1,2,NPORT))/(GNI(2,1,NPORT)*ZOUT
     #+GNI(2,2,NPORT))


C     ON-OFF STATE
      ZIN = ZINON*ZINOFF/(ZINON+ZINOFF)
      VIN = ZIN*VS/(ZIN+ZS)
      IIN  =  VIN/ZIN
      PIN  =  REAL(.5*(VIN*DCONJG(IIN)))
      ION  =  IIN*ZINOFF/(ZINON+ZINOFF)
      IOFF = IIN - ION
      PON  = 0.5*REAL(VIN*DCONJG(ION))
      POFF = 0.5*REAL(VIN*DCONJG(IOFF))
      ILON = GPI(1,1,NPORT)*ION-GPI(2,1,NPORT)*VIN
      VLON = GPI(2,2,NPORT)*VIN-GPI(1,2,NPORT)*ION
      PLON = PON-0.5*REAL(VIN*DCONJG(ION)-VLON*DCONJG(ILON))
      AMP  = PEX/PLON
      WRITE(2,55) FRE
      WRITE(2,60) Q
      WRITE(2,65) ND
      WRITE(2,70) CJ
      WRITE(2,75) RR
      WRITE(2,80) PIN*AMP
      WRITE(2,85) PON*AMP
      WRITE(2,90) POFF*AMP
      WRITE(2,95) PLON*AMP
      ILOFF = GNI(1,1,NPORT)*IOFF-GNI(2,1,NPORT)*VIN
      VLOFF = GNI(2,2,NPORT)*VIN -GNI(1,2,NPORT)*IOFF
      PLOFF = POFF-0.5*REAL(VIN*DCONJG(IOFF)-VLOFF*DCONJG(ILOFF))
      WRITE(2,100) PLOFF*AMP
55    FORMAT(' ','OPERATING FREQUENCY',3X,F5.2,2X,'GHZ')
60    FORMAT(' ','FIGURE OF MERIT (DIODE Q)',3X,F8.3)
65    FORMAT(' ','TOTAL NUMBER OF DIODE IN EACH BRANCH',2X,I2)
70    FORMAT(' ','DIODE JUNCTION CAPACITANCE',3X,F5.3,2X,'PF')
75    FORMAT(' ','DIODE JUNCTION RESISTANCE',3X,F5.3,2X,'OHM')
80    FORMAT(' ','INPUT POWER',F10.2,3X,'WATTS')
85    FORMAT(' ','POWER IN ON STATE BRANCH',2X,F10.2,3X,'WATTS')
90    FORMAT(' ','POWER IN OFF STATE BRANCH',1X,F10.2,3X,'WATTS')
95    FORMAT(' ','POWER DELIVER TO THE LOAD IN ON STATE',F10.2,3X,'WATTS
     *')
100   FORMAT(' ','POWER DELIVER TO THE LOAD IN OFF STATE',F10.6,3X,'WATT
     *S')


C     POWER DISSIPATED IN ON STATE BRANCH
      VON = VIN
      CALL POWER(GP(1,1,1),ION,VON,NPORT,PDON,IDON,VDON)
      WRITE(2,*)'POWER DISSIPATION IN DIODE ON STATE'
      DO 105 I = 2,2*ND,2
      WRITE(2,115)I/2,PDON(I)*AMP
105   CONTINUE

C     POWER DISSIPATED IN OFF STATE BRANCH
      VOFF = VIN
      CALL POWER(GN(1,1,1),IOFF,VOFF,NPORT,PDOFF,IDOFF,VDOFF)
      WRITE(2,*)'POWER DISSIPATION IN DIODE OFF STATE'
      DO 110 J = 2,2*ND,2
      WRITE(2,115)J/2,PDOFF(J)*AMP
110   CONTINUE
115   FORMAT(' ','POWER DISSIPATED IN DIODE NO.',1X,I2,2X,F10.5,2X,'WATT
     *S')

C     JUNCTION TEMPERATURE CALCULATION
C     JUNCTION TEMPERATURE IN ON STATE BRANCH
```

```
      IF(TYPE.EQ.'N')STOP
      IF(TYPE.EQ.'C')THEN
      CALL THERM1(ND,TJON,PDON,AMP,TA,TR)
      ELSE
      CALL THERM2(ND,TJON,PDON,AMP,TA,DT,HC)
      ENDIF
      WRITE(2,*)'JUNCTION TEMPERATURE ON STATE BRANCH'
      DO 120 I = 1,ND
      WRITE(2,82)I,TJON(I)
120   CONTINUE
C     JUNCTION TEMPERATURE IN OFF STATE BRANCH
      WRITE(2,*)'JUNCTION TEMPERATURE OFF STATE BRANCH'
      IF(TYPE.EQ.'C')THEN
      CALL THERM1(ND,TJOFF,PDOFF,AMP,TA,TR)
      ELSE
      CALL THERM2(ND,TJOFF,PDOFF,AMP,TA,DT,HC)
      ENDIF
      DO 125 J = 1,ND
      WRITE(2,130)J,TJOFF(J)
125   CONTINUE
130   FORMAT(' ','JUNCTION TEMPERATURE DIODE NO.',2X,I2,2X,F6.2,2X,'DEGR
     *EE C')
      STOP
      END



c                          SUBROUTINE MATRIX
      SUBROUTINE MATRIX(RR,CJ,Z,EL,NSEG,ND,FRE,GP)
      REAL*8 RR,CJ,EL(10),FRE,PI
      COMPLEX*16 Z(10),Z1
      COMPLEX*16 G(2,2,20),G1(2,2,20),GP(2,2,20)
      PI = 3.1415926536
      DO 10 K = 1,NSEG
      G(1,1,K) = DCMPLX(COS(EL(K)),0.D0)
      G(1,2,K) = DCMPLX(0.D0,1.D0)*Z(K)*DCMPLX(SIN(EL(K)),0.D0)
      G(2,1,K) = DCMPLX(0.D0,1.D0)/Z(K)*DCMPLX(SIN(EL(K)),0.D0)
      G(2,2,K) = G(1,1,K)
10    CONTINUE
      DO 20 L=1,ND
      IF(CJ.EQ.0.D0)THEN
      Z1 = DCMPLX(RR,0.D0)
      ELSE
      Z1 = DCMPLX(RR,-1000/(2*PI*FRE*CJ))
      ENDIF
      G1(1,1,L) = DCMPLX(1.D0,0.D0)
      G1(1,2,L) = DCMPLX(0.D0,0.D0)
      G1(2,1,L)= 1/Z1
      G1(2,2,L) = G1(1,1,L)
20    CONTINUE
      DO 30 M =1,NSEG
      N = 2*M-1
      GP(1,1,N) = G(1,1,M)
      GP(1,2,N) = G(1,2,M)
      GP(2,1,N) = G(2,1,M)
      GP(2,2,N) = G(2,2,M)
30    CONTINUE
      DO 40 I =1,ND
      J = 2*I
      GP(1,1,J) = G1(1,1,I)
      GP(1,2,J) = G1(1,2,I)
      GP(2,1,J) = G1(2,1,I)
      GP(2,2,J) = G1(2,2,I)
40    CONTINUE
      RETURN
      END
```

```
c                                SUBROUTINE MATMUL
      SUBROUTINE MATMUL(AA,BB,NN,MM,RR,CC)
      INTEGER NN,MM,RR
      COMPLEX*16 AA(2,2,1),BB(2,2,1),CC(2,2,1)
      DO 10 I = 1,NN
      DO 20 J = 1,RR
      CC(I,J,1) = 0
      DO 30 K =1,MM
      CC(I,J,1) = CC(I,J,1) + AA(I,K,1)*BB(K,J,1)
30    CONTINUE
20    CONTINUE
10    CONTINUE
      RETURN
      END


c                                SUBROUTINE POWER
      SUBROUTINE POWER(G,I,V,N,PD,IID,VID)
      REAL*8 PD(10)
      COMPLEX*16 G(2,2,20),V,I,IID(20),VID(20),IOD(20),VOD(20)
      DO 10 J=2,N,2
      IID(J) = G(1,1,J-1)*I - G(2,1,J-1)*V
      VID(J) = G(2,2,J-1)*V - G(1,2,J-1)*I
      IOD(J) = G(1,1,J)*IID(J) - G(2,1,J)*VID(J)
      VOD(J) = G(2,2,J)*VID(J) - G(1,2,J)*IID(J)
      PD(J)  = 0.5*REAL(VID(J)*DCONJG(IID(J))-VOD(J)*DCONJG(IOD(J)))
      I = IOD(J)
      V = VOD(J)
10    CONTINUE
      RETURN
      END


c                                SUBROUTINE THERM1
      SUBROUTINE THERM1(ND,TJ,PD,AMP,TA,TR)
      INTEGER ND
      REAL TJ(10),AMP,TA,TR
      REAL*8 PD(10)
      DO 5 I=1,ND
      TJ(I) = TA + (PD(I*2)*AMP)*TR
5     CONTINUE
      RETURN
      END


c                                SUBROUTINE THERM2
      SUBROUTINE THERM2(ND,TJ,PD,AMP,TA,DT,HC)
      INTEGER ND
      REAL TJ(10),AMP,TA,DT,HC
      REAL*8 PD(10)
      DO 5 J =1,ND
      TJ(J) = TA + (PD(J*2)*AMP)*DT/HC
5     CONTINUE
      RETURN
      END
```

LIST OF REFERENCES

1. Kurokawa, K. and Schlosser, O., "Quality Factor of Switching Diodes for Digital Modulation," *Proc. IEEE*, v. 38, p. 180, 1970.

2. Atwater, H. and Sudbury, R., "Use of Switching Q in The Design of FET Microwave Switches," *IEEE Sympos. Microwave Theory Tech.*, p. 377, 1981.

3. Kawakami, S., "Figure of Merit Associated with A Variable Parameter One-port for RF Switching and Modulation," *IEEE Trans. Circuit Theory*, v. CT-12, p. 321, 1965.

4. Hines, M., "Fundamental Limitation in R.F. Switching and Phase Shifting Using Semiconductor Diodes," *Proc. IEEE*, v. 52, p. 697, 1954.

5. Brown, R. G., Sharpe, R. A., Hughes, W. L., and Post, R. E., *Lines, Waves, and Antennas The Transmission of Electric Energy*, John Wiley & Sons, New York, 1973.

6. Matthews, P. A. and Stephenson, I. M. , *Microwave Components*, Chapman and Hall Ltd, London, 1968.

7. White, J. F., *Microwave Semiconductor Engineering*, Van Nostand Reinhold Company, New York, 1982.

8. Cheng, D. K., *Field and Wave Electromagnetics*, Addison-Wesley Publishing Company, Inc., Massachusetts, 1983.

9. *PIN Diode Designers Guide*, Microwave Associates Company, Maryland, 1982.

10. Watson H. A., *Microwave Semiconductor Devices and Their Circuit Application*, McGraw-Hill Book Company, New York, 1969.

11. Guild, J., Rein, S., and Skogrand, L., *Touchstone Reference Manual Version 1.5*, EEosf, Inc., 31194 La Baya Drive, Westlake Village, California, 91362, 1987.

12. Holmes, C., and Morton, D., "Determination of Node within A Circuit," *EEsof Application Note 2*, EEsof Inc., Westlake Village, California, 1985.

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